

A Novel 13-Level Switched-Capacitor Multilevel Inverter Architecture

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Abstract

This article introduces a novel 13-level switched-capacitor multilevel inverter (13LSCMLI) architecture with a sextuple voltage boosting capacity using a single DC supply, 12 switches, 2 diodes, and 3 capacitors. Achieving a sextuple voltage gain makes it suitable for photovoltaic systems. Self-voltage balancing of the capacitors is accomplished without the necessity of intricate control systems or additional circuits. To produce negative polarity, the suggested architecture does not require an H-bridge, reducing the voltage stresses across the switches. Thus, the total standing voltage of the suggested architecture is comparable to other topologies reported in the literature. The voltage stress across the switches is limited to six times the input DC voltage. One major benefit of the suggested 13-level inverter over alternative arrangements is its reduced cost function value. A 13-level simulation model of the presented switched-capacitor topology is designed using the nearest level control modulation scheme. To determine the efficiency, conduction losses, and switching losses of the presented 13-level SCMLI, a power loss study is performed using PLECS software. Simulation results of the presented architecture are compared with other recent 13-level topologies under various parameters. Ultimately, simulation outcomes derived under specific loading and modulation index scenarios demonstrate the effectiveness of the presented architecture. Experimental investigations conducted under various scenarios confirm the accuracy of the simulation results.

Categories: Power Electronics and Renewable Energy

Keywords: switched-capacitor, multilevel inverters, nearest level control, sextuple voltage boost, total standing voltage

Introduction

Over the past few decades, multilevel inverters (MLIs) have been used owing to benefits like higher electromagnetic compatibility, lower dv/dt stress on active switches, better power quality, and the capability to function at variable switching frequencies [1]. The three conventional MLIs are the cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC) topologies [2]. FC and NPC use a single DC source, while CHB uses multiple DC sources for the generation of output voltage levels [3-5]. These architectural configurations are complicated and expensive since they require a large number of components. For instance, NPC fails to achieve neutral point balancing, FC requires several flying capacitors with complex voltage balancing, and CHB has numerous independent DC voltage sources [6]. Due to their simplicity and adaptability, cascaded H-bridges are the most frequently used topologies in the existing literature [7]. These traditional MLIs have the disadvantage of having more switches, as well as lacking the ability to self-balance and boost voltage for higher voltage levels [8].

To overcome the drawbacks of conventional MLIs, various topologies have been presented over the last two decades. Modern MLI topologies strive for reduced total standing voltage (TSV), fewer DC voltage sources, and fewer switches. In the literature, several lower-count topologies have been considered under these constraints [9]. Among the various other

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reduced-switch topologies, the switched-capacitor multilevel inverter (SCMLI) topology requires fewer switches and driver circuits, and because capacitors serve as backup DC sources, it requires fewer DC power supplies, which results in a more compact design and lower costs. In SCMLI, capacitors are used as DC sources with sequential charging and discharging. Capacitor voltages are self-balanced, thus reducing the circuit complexity [10-12].

Due to the above-mentioned advantages of SCMLI, various MLI structures have been presented in the literature. Considering 13-level (13L) topologies, the authors in [13] propose a 13L switched-capacitor topology with thirteen switches and three capacitors that has the lowest efficiency. Authors in [14] developed a 13L topology having a maximum blocking voltage (MBV) equal to 3 at the cost of a higher number of components and only a triplen voltage gain. The 13L topology presented in [15] has a sextuple voltage gain, but the total number of components is higher. The topology demonstrated by the authors in [16] has the least MBV at the expense of a higher number of switches. By using 13 switches, the authors in [17] present a sextuple-boost 13L inverter. The architecture presented by the authors in [18] has a high-efficiency 13L inverter, but the cost function (CF) value is high, and the achieved voltage gain is only 1.5. Authors in [19] present a reduced-switch 13L inverter structure, but four capacitors are required for generating the output. The topologies presented in [20-22] use dual DC sources to generate a 13L output.

Thus, switch stress, the number of switches, the number of capacitors, and voltage gain all play important roles in the optimal selection of an inverter. Keeping these points in mind, this article presents a novel 13-level switched-capacitor multilevel inverter (13LSCMLI) architecture. The presented architecture has the following features.

- The presented architecture generates a 13-level output voltage with a sextuple voltage boosting feature using a single DC source, 12 switches, 2 diodes, and 3 self-balanced capacitors.
- Four pairs of switches are complementary, thus reducing the requirement for driver circuits and circuit complexity.
- Capacitor voltages are self-balanced; therefore, no additional sensors are required to balance the capacitor voltages.

Materials And Methods

Presented 13LSCMLI architecture

Architecture Description

The circuit configuration of the presented 13LSCMLI architecture uses 12 switches (S_1 to S_{12}), 3 capacitors (C_1 to C_3), 2 diodes (D_1 to D_2) and 1 DC input (V_{DC}), as shown in Figure 7. The voltages of the capacitors are self-regulated by charging in parallel while discharging in series according to the desired voltage. Table 1 and Figure 2 show the switching sequence and the graphical representation of the states for each output voltage during the positive and negative half-cycles, respectively. The output voltage levels are generated as $\pm 0V_{DC}$, $\pm V_{DC}$, $\pm 2V_{DC}$, $\pm 3V_{DC}$, $\pm 4V_{DC}$, $\pm 5V_{DC}$, and $\pm 6V_{DC}$. Capacitors C_1 , C_2 , and C_3 charge in the ratio of 1:1:3 V_{DC} by sequentially turning the switches ON and OFF in each cycle to achieve a voltage gain of 6. It is worth noting from Table 1 that the switch pairs (S_1 - S_2), (S_3 - S_4), (S_9 - S_{10}), and (S_{11} - S_{12}) are complementary to each other, which reduces the circuit complexity.

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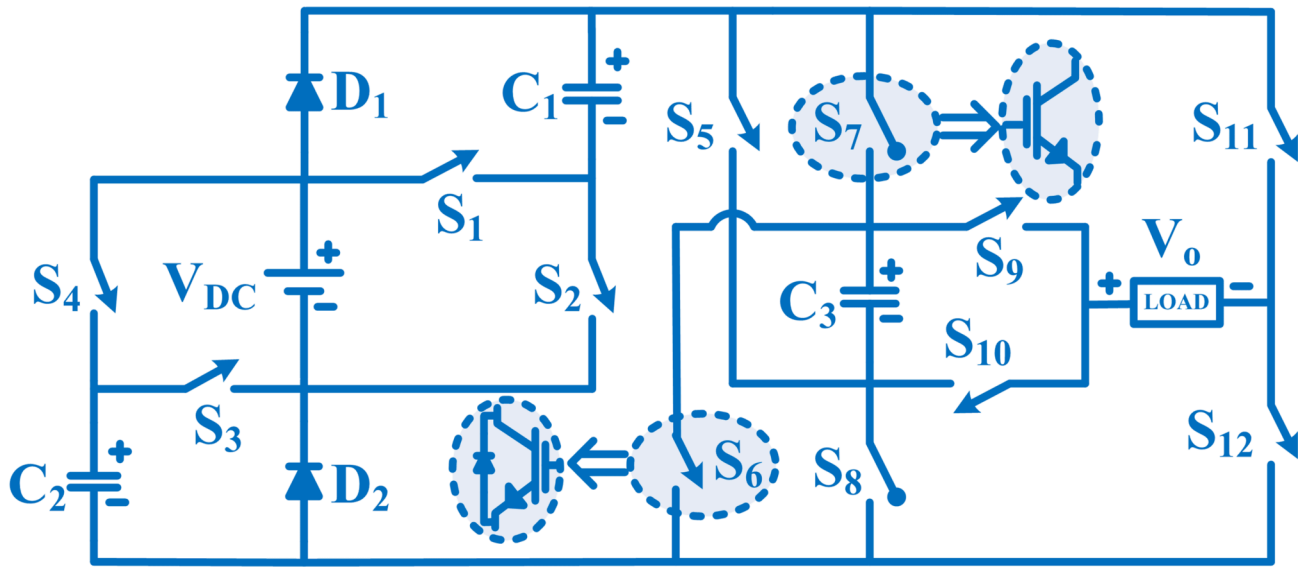


FIGURE 1: Circuit configuration of the presented 13LSCMLI architecture

13LSCMLI, 13-level switched-capacitor multilevel inverter

Operating States

Different switching states of operation are discussed below:

State 1: In state 1, V_{DC} and three capacitors (C_1 , C_2 and C_3) are connected in series, giving $+6V_{DC}$ at the output. In this state, all the capacitors are discharged, as displayed in Figure 2A.

State 2: In state 2, V_{DC} and two capacitors (C_1 and C_3) are discharged and connected in series, giving $+5V_{DC}$ at the output as displayed in Figure 2B. Simultaneously, capacitor C_2 charges to V_{DC} .

State 3: In state 3, capacitor C_3 gets discharged in series with the source V_{DC} as displayed in Figure 2C in order to produce $+4V_{DC}$ at the output. Simultaneously, capacitors C_1 and C_2 are charged to V_{DC} in parallel with the source.

State 4: In state 4, an output level of $+3V_{DC}$ is achieved by discharging capacitors C_1 and C_2 in series with the source. Simultaneously, capacitor C_3 is charged in parallel with the source, as displayed in Figure 2D.

State 5: In state 5, an output level of $+2V_{DC}$ is achieved by discharging capacitor C_1 in series with the source. Simultaneously, capacitor C_2 is charged in parallel with the source as displayed in Figure 2E. Capacitor C_3 remains in the idle state.

State 6: In state 6, capacitors C_1 and C_2 charge to V_{DC} while capacitor C_3 remains in the idle state as displayed in Figure 2F. An output level of $+1V_{DC}$ is achieved by connecting the load in series with the source.

State 7: In state 7, capacitors C_1 and C_2 discharge to V_{DC} to produce the $+0V_{DC}$ at the output, while capacitor C_3 charges in parallel with the series combination of the source and capacitors C_1 and C_2 as displayed in Figure 2G.

State 8: In state 8, capacitor C_1 and C_2 discharge to V_{DC} to produce the $-0V_{DC}$ at the output while capacitor C_3 charges in parallel with the series combination of the source, capacitor C_1 and C_2 as displayed in Figure 2H.

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State 9: In state 9, capacitor C_1 and C_2 charge to V_{DC} while capacitor C_3 remains in the idle state as displayed in Figure 2I. An output level of $-1V_{DC}$ is achieved by turning on the switches S_6 , S_9 and S_{11} in series with the source and load.

State 10: In state 10, an output level of $-2V_{DC}$ is achieved by discharging capacitor C_1 in series with the source and by turning on switches S_6 , S_9 , and S_{11} . Simultaneously, capacitor C_2 is charged in parallel with the source as displayed in Figure 2J. Capacitor C_3 remains in the idle state.

State 11: In state 11, an output level of $-3V_{DC}$ is achieved by discharging capacitor C_1 and C_2 discharged in series with the source while turning on the switches S_8 , S_{10} , and S_{11} . Simultaneously, capacitor C_3 is charged in parallel with the source as displayed in Figure 2K.

State 12: In state 12, capacitor C_3 is discharged in series with the source V_{DC} by turning on the switches S_6 , S_{10} , and S_{11} as displayed in Figure 2L in order to produce $-4V_{DC}$ at the output. Simultaneously, capacitors C_1 and C_2 are charged to V_{DC} in parallel with the source.

State 13: In state 13, V_{DC} and two capacitors (C_1 and C_3) are discharged, connected in series, and by turning on the switches S_6 , S_{10} , and S_{11} produce $-5V_{DC}$ at the output, as displayed in Figure 2M. Simultaneously, capacitor C_2 charges to V_{DC} .

State 14: In state 14, V_{DC} and three capacitors (C_1 , C_2 , and C_3) are connected in series, and, by turning on the switches S_6 , S_{10} , and S_{11} produce $-6V_{DC}$ at the output. In this state, all the capacitors are discharged as displayed in Figure 2N.

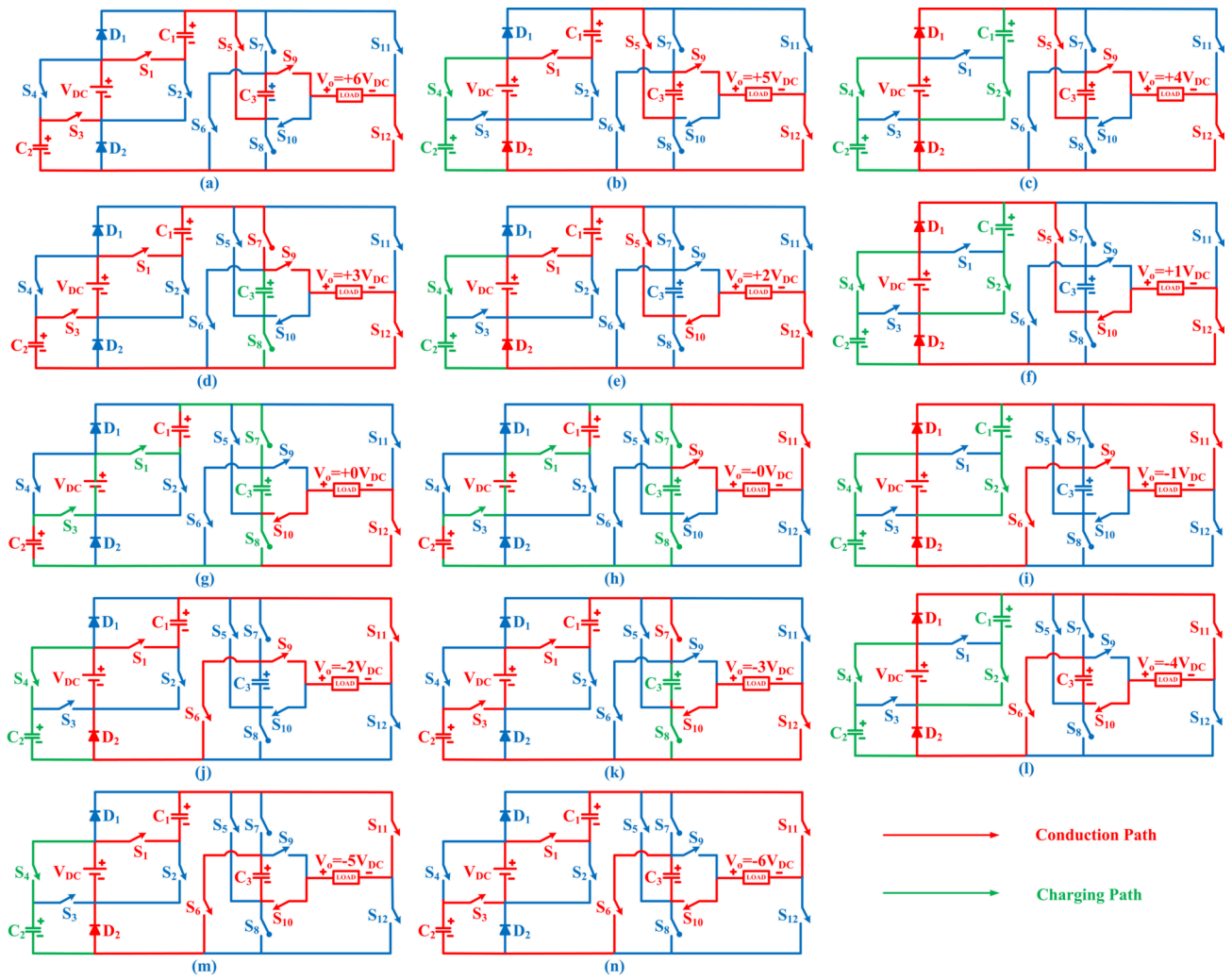


FIGURE 2: ON and OFF states of the presented architecture: (a-g) positive half-cycle and (h-n) negative half-cycle

State	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	C ₁	C ₂	C ₃	D ₁	D ₂	Output Voltage
1	1	0	1	0	1	0	0	0	1	0	0	1	D	D	D	0	0	+6 V _D C
2	1	0	0	1	1	0	0	0	1	0	0	1	D	C	D	0	1	+5 V _D C
3	0	1	0	1	1	0	0	0	1	0	0	1	C	C	D	1	1	+4 V _D C
4	1	0	1	0	0	0	1	1	1	0	0	1	D	D	C	0	0	+3 V _D C
5	1	0	0	1	1	0	0	0	0	1	0	1	D	C	I	0	1	+2 V _D C
6	0	1	0	1	1	0	0	0	0	1	0	1	C	C	I	1	1	+1 V _D C
7	1	0	1	0	0	0	1	1	0	1	0	1	D	D	C	0	0	+0 V _D C
8	1	0	1	0	0	0	1	1	1	0	1	0	D	D	C	0	0	-0V DC
9	0	1	0	1	0	1	0	0	1	0	1	0	C	C	I	1	1	-1V DC
10	1	0	0	1	0	1	0	0	1	0	1	0	D	C	I	0	1	-2V DC
11	1	0	1	0	0	0	1	1	0	1	1	0	D	D	C	0	0	-3V DC

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12	0	1	0	1	0	1	0	0	0	1	1	0	C	C	D	1	1	-4V DC
13	1	0	0	1	0	1	0	0	0	1	1	0	D	C	D	0	1	-5V DC
14	1	0	1	0	0	1	0	0	0	1	1	0	D	D	D	0	0	-6V DC

TABLE 1: Switching states transitioning for the 13-level inverter architecture

1, ON; 0, OFF; C, Charging; D, Discharging; I, Idle

Selection of Capacitor Value and Capacitor Self-Voltage Balance

The intervals of time when C_1 , C_2 , and C_3 are charged and discharged are illustrated in Figure 3. The highest discharging period (HDP) of the capacitors is used to determine the best capacitor value [16]. In Figure 3, HDP for C_1 , C_2 , and C_3 are (t_5-t_5') , (t_6-t_6') , and (t_4-t_4') , respectively. The amount of discharge during the HDP for capacitors C_1 , C_2 , and C_3 can be calculated by Equation (1).

$$\Delta Q_C^{(j)}, j = 1, 2, 3 = (1/2\pi f_0) \int_{t_k}^{t_k'} i_o(t) dt, \quad k = 5, 6, 4$$

The time instants t_4 , t_5 , t_6 , t_4' , t_5' and t_6' can be calculated as (2) and (3) respectively.

$$t_{k=4,5,6} = \frac{\sin^{-1}\left(\frac{2k-1}{12}\right)}{2\pi f_0}$$

$$t'_{k=4,5,6} = \frac{\pi - \sin^{-1}\left(\frac{2k-1}{12}\right)}{2\pi f_0}$$

where f_0 is the fundamental output frequency. The output current during HDP for a resistive load may be written as Equations (4), (5), and (6).

$$i_o(t) = \frac{4V_{DC}}{R_L}, \quad t_4 < t < t_5$$

$$i_o(t) = \frac{5V_{DC}}{R_L}, \quad t_5 < t < t_6$$

$$i_o(t) = \frac{6V_{DC}}{R_L}, \quad t_6 < t < \frac{T}{4}$$

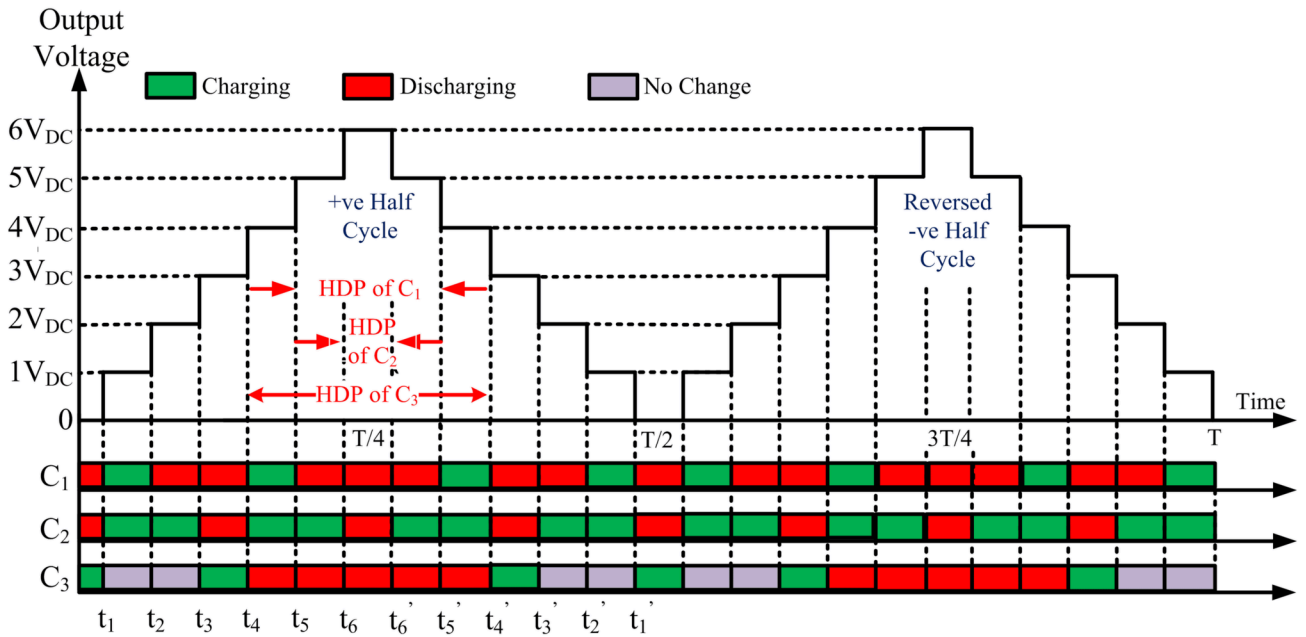


FIGURE 3: 13-Level output voltage showing HDPs of capacitors

HDP, highest discharging period

With the help of (1)-(6), C_1 , C_2 , and C_3 are calculated as Equation (7)

$$C_n = \frac{\Delta Q_{C_n}}{\Delta V_{C_n}(\%) V_{C_n}}$$

where, V_{C_n} represents the voltage across the n^{th} capacitor while ΔV_{C_n} is the percentage allowable voltage ripple. By taking the permissible value of ΔV_{C_n} as 10% of the input DC voltage and for a load of 100Ω, the most suitable values of capacitors C_1 , C_2 , and C_3 are 1180 μF, 762 μF, and 1,371 μF, respectively, for simulation. For the experimental setup, all the capacitors were chosen as 2,200 μF.

When all three capacitors are linked in parallel to the source and in series with the load at various times, their voltages self-balance to the proper values. This permits the capacitors to maintain the desired voltage levels. Because the charging loop's time constant and total parasitic resistance are very low, there is always adequate time for the capacitors to charge completely, regardless of voltage levels. Figure 10, shows that the capacitor voltages remain balanced throughout the fundamental cycle within permissible ripple values.

Total Standing Voltage (TSV)

TSV represents the sum of the maximum blocking voltage (MBV) across the switches and is described as

$$\text{TSV}_{\text{p.u.}} = \frac{\sum_{m=1}^{12} V_{SW,m} + \sum_{n=1}^2 V_{D,n}}{V_{o,m}}$$

where, $V_{SW,m}$ and $V_{D,n}$ represent the MBV of each switch and diode, respectively, and $V_{o,m}$ is the maximum value of output voltage. Each switch has its MBV specified as

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{D1} = V_{D2} = 1V_{DC}$$

$$V_{S7}=V_{S8}=V_{S9}=V_{S10}=V_{S11}=V_{S12}=3V_{DC}$$

$$V_{S5}=V_{S6}=6V_{DC}$$

Voltage stresses on different components for each output voltage level is also shown in Figure 4.

$$TSV=V_{S1}+V_{S2}+V_{S3}+V_{S4}+V_{S5}+V_{S6}+V_{S7}+V_{S8}+V_{S9}+V_{S10}+V_{S11}+V_{S12}+V_{D1}+V_{D2}=36V_{DC}$$

$$TSV_{p,u} \text{ is given as, } TSV_{p,u}=36/6=6$$

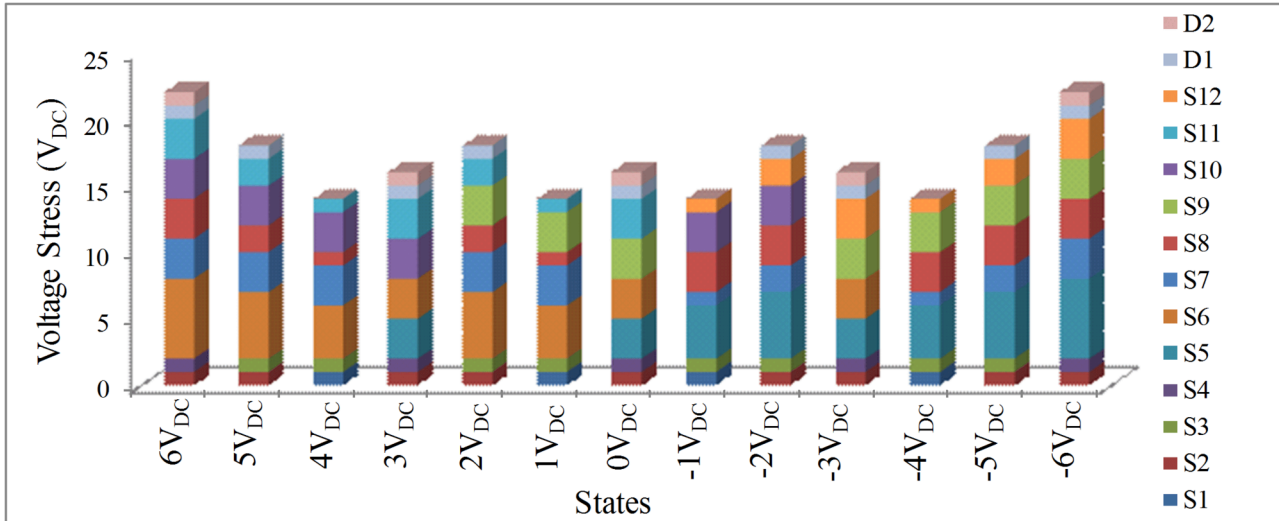
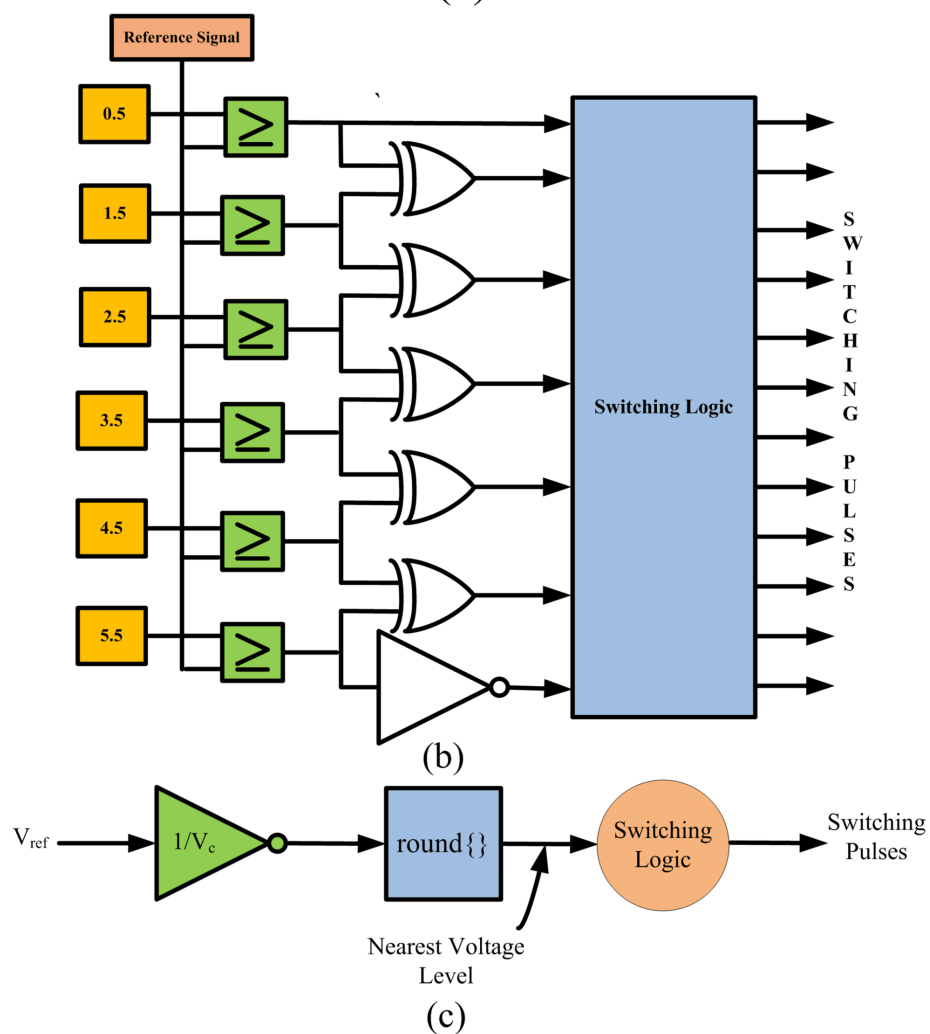
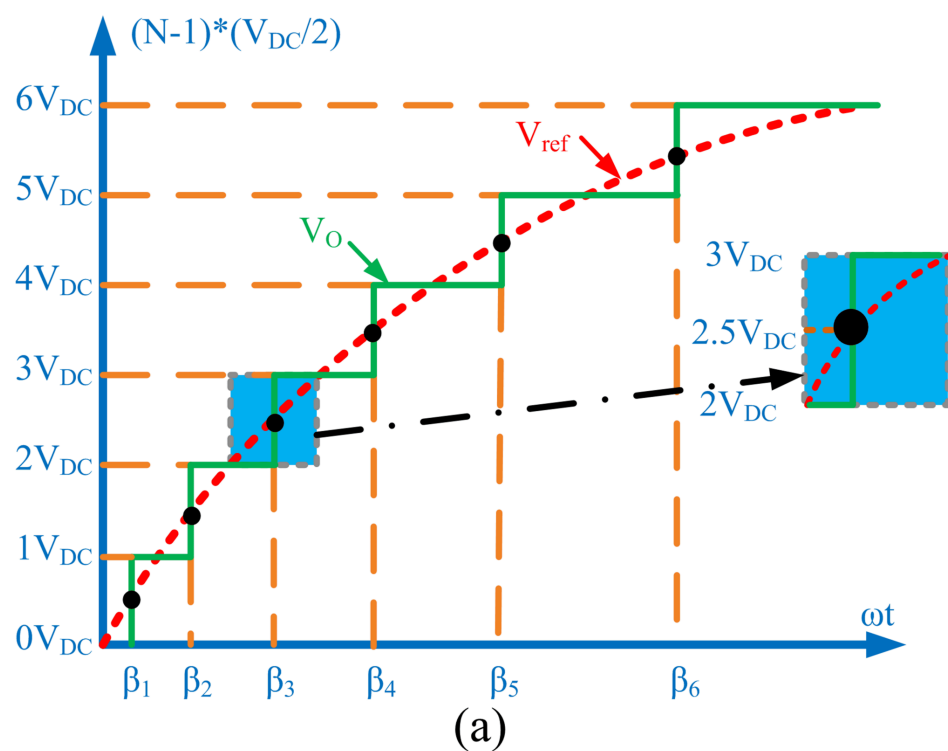


FIGURE 4: Voltage stresses on different components for each output level

Modulation Strategy

In this work, one of the low switching frequency modulation schemes i.e. Nearest Level Control (NLC) is used, operating at a 50 Hz switching frequency. In the NLC scheme, the output voltage level changes when the reference sinusoidal waveform value of $((N-1)/2)V_{DC}$, where N is the number of output voltage levels, crosses the constant DC values of 0.5, 1.5, 2.5, ... depending upon the number of voltage levels. When the value of the reference sinusoidal waveform becomes greater than the constant values of 0.5 and 1.5, the voltage level changes from 0 to V_{DC} and from V_{DC} to $2V_{DC}$, respectively, to obtain a sampled waveform. Afterwards, the resulting waveform is rounded to the closest integer and compared according to the switching logic provided in Table 1 in order to create switching signals for the associated IGBTs [14]. In a similar manner, every output voltage level is produced as shown in Figure 5A. The control logic and control diagram for switching pulse generation for the positive half-cycle are shown in Figure 5B and Figure 5C. For the negative half-cycle, the reference signal is reversed using a NOT gate, and logic signals are generated in a similar manner based on the switching table (Table 1).



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FIGURE 5: (a) NLC level generation method; (b) control logic for switching pulse generation; (c) control diagram

NLC, Nearest Level Control

Results And Discussion

Power losses and efficiency

Power loss in converters mostly occurs as conduction losses (P_{CL}), switching losses (P_{SL}), and voltage ripple losses (P_{VRL}) in capacitors [20].

Switching Losses

Switching loss mainly occurs due to the turning on (t_{on}) and turning off (t_{off}) of switches. The switching losses of the conducting switches are derived by Equations (9-11)

$$P_{on} = \frac{1}{6} f_{sw} V_o I_o t_{on} \quad (9)$$

$$P_{off} = \frac{1}{6} f_{sw} V_{off} I_{off} t_{off} \quad (10)$$

$$P_{SL} = \sum_{k=1}^{12} \left(\sum_{i=1}^{N_{on,k}} P_{on,k,i} + \sum_{i=1}^{N_{off,k}} P_{off,k,i} \right) \quad (11)$$

where, t_{on} and t_{off} are the switch's on and off times, respectively. i_{on} is the current flowing through the switch when the switch is turned on completely, i_{off} is the current flowing through the switch just before it turns off, V_{off} is the voltage of the n^{th} switch when it is in off condition, f_{sw} is the switching frequency, $N_{on,k}$ and $N_{off,k}$ are the device on/off stages count, respectively.

Conduction Losses

Conduction losses occur due to the on-state resistance of the switches and body diodes. Conduction losses are derived by (12), where $P_{CL,S}$, $P_{CL,D}$, and $P_{CL,C}$ are conduction loss of switches, diodes and capacitors, respectively.

$$P_{CL} = P_{CL,S} + P_{CL,D} + P_{CL,C} \quad (12)$$

Voltage Ripple Loss of Capacitors

Voltage ripple loss of capacitor is another source of loss which can be computed from (13), where f_{sw} : switching frequency, C_n : capacitance of the n^{th} capacitor, $\Delta V_{ripple,n}$: ripple voltage of n^{th} capacitor.

$$P_{loss,ripple} = \frac{1}{2} f_{sw} C_n (\Delta V_{ripple,n})^2 \quad (13)$$

Efficiency Calculation

Efficiency (η) of the presented 13 architecture is determined using (14).

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$$\eta = \left(\frac{\text{Output Power}}{\text{Output Power} + \text{Losses}} \right) \times 100 \quad (14)$$

Power loss and efficiency of the presented architecture is analyzed by thermal modelling using PLECS software. The IKY75N120CH3_IGBT thermal model of switch is taken for the loss calculations. Figure 6 shows the thermal model plot of turn-on, turn-off and conduction losses at 25°C and 175°C. Figure 7 displays the distribution of conduction and switching losses for different components at a 500 W output power. Also, an efficiency curve is drawn in Figure 8 for different values of output power ranging from 100 W to 1,000 W.

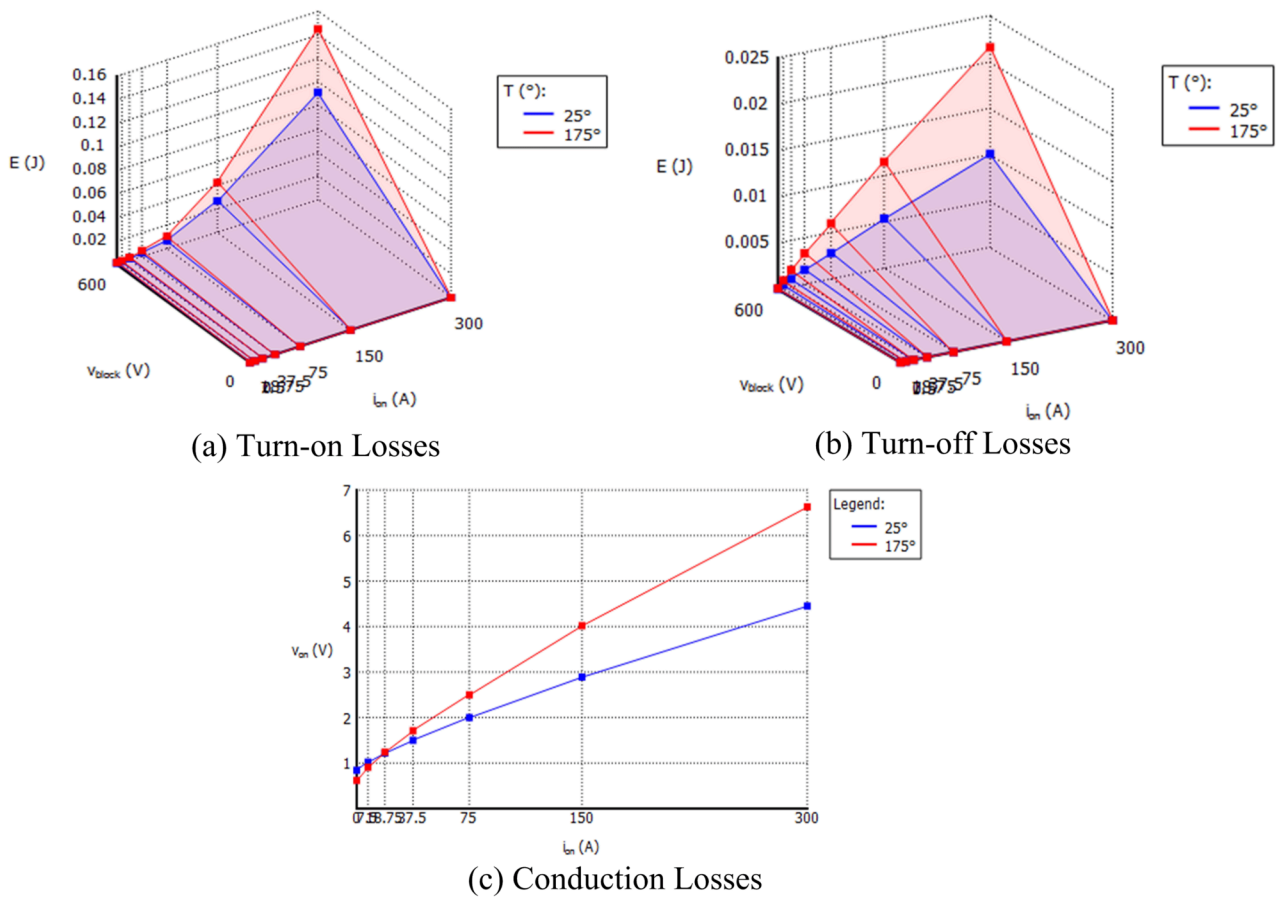


FIGURE 6: IGBT(IKY75N120CH3) thermal model: (a) Turn-ON loss; (b) Turn-OFF loss; (c) Conduction loss

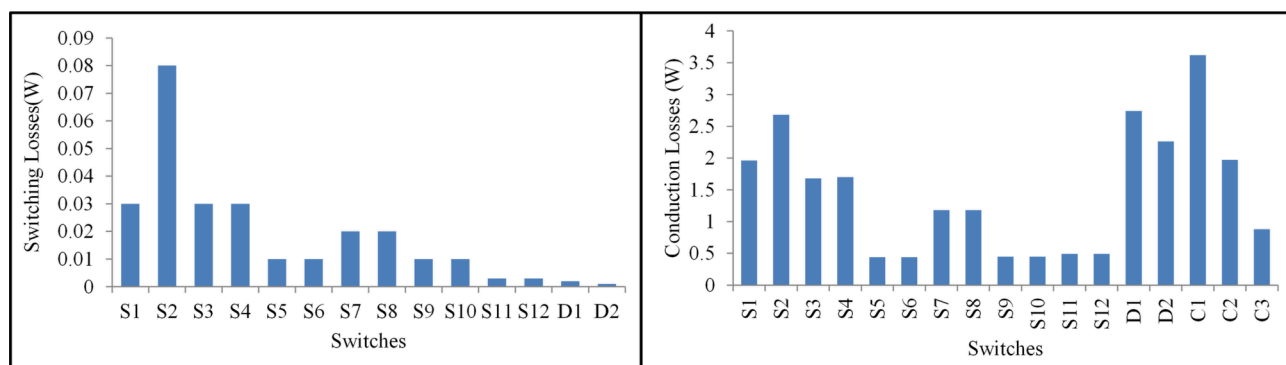


FIGURE 7: Conduction and switching loss distribution for different components

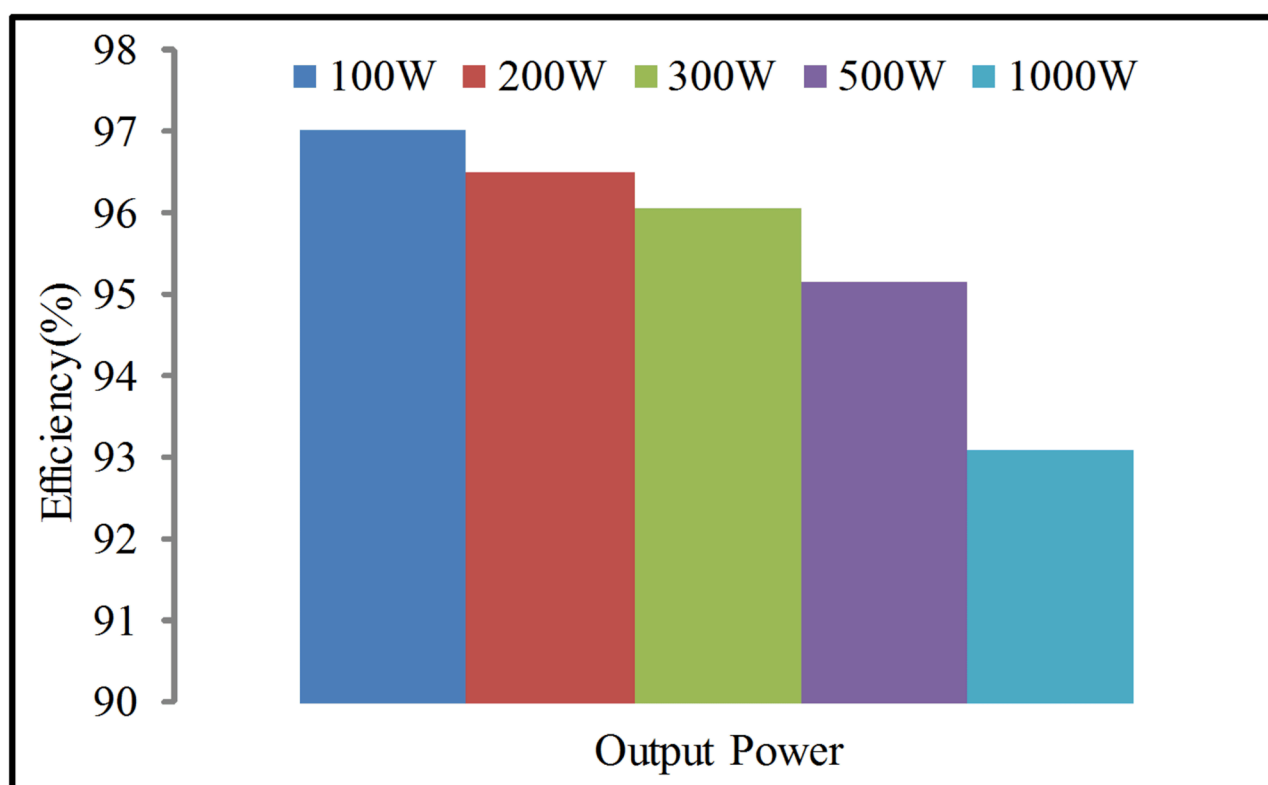


FIGURE 8: Efficiency vs output power

Comparable Evaluation

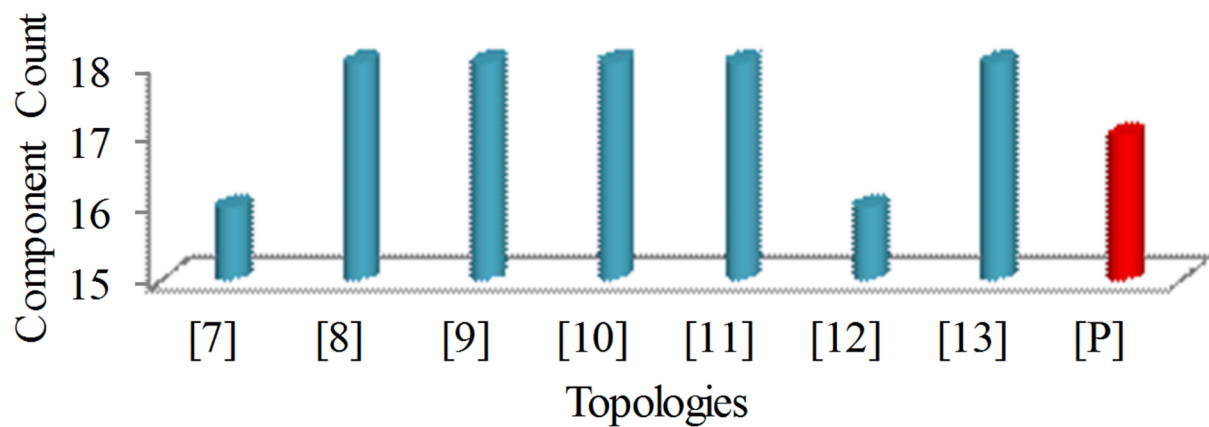
Table 2 compares the presented 13LSCMLI design to various single-source 13-level contemporary topologies to evaluate its pros and cons. The switch count and the number of gate drivers in the presented topology are lower than those of the other counterparts except for that in the study [19], at the cost of one extra capacitor and diode. The number of components per level of the presented architecture is also lower, except for that of the research [13] and [18], although the TSV_{pu} of the presented architecture is in line with the existing topologies. The presented architecture is also compared on the basis of another important parameter called the cost function (CF).

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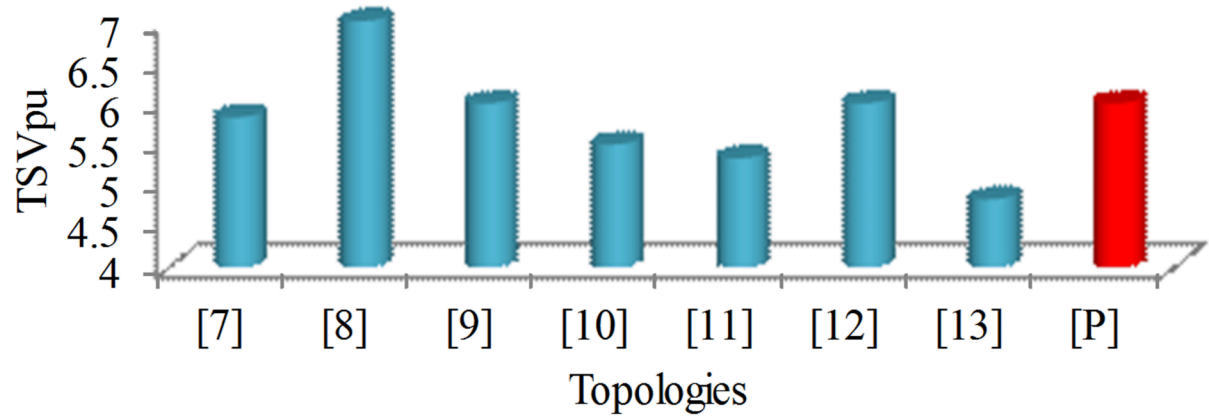
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$$CF = (N_{sw} + N_D + N_C + \sigma TSV_{pu}) \times \frac{N_{DC}}{\text{Gain}} \quad (15)$$

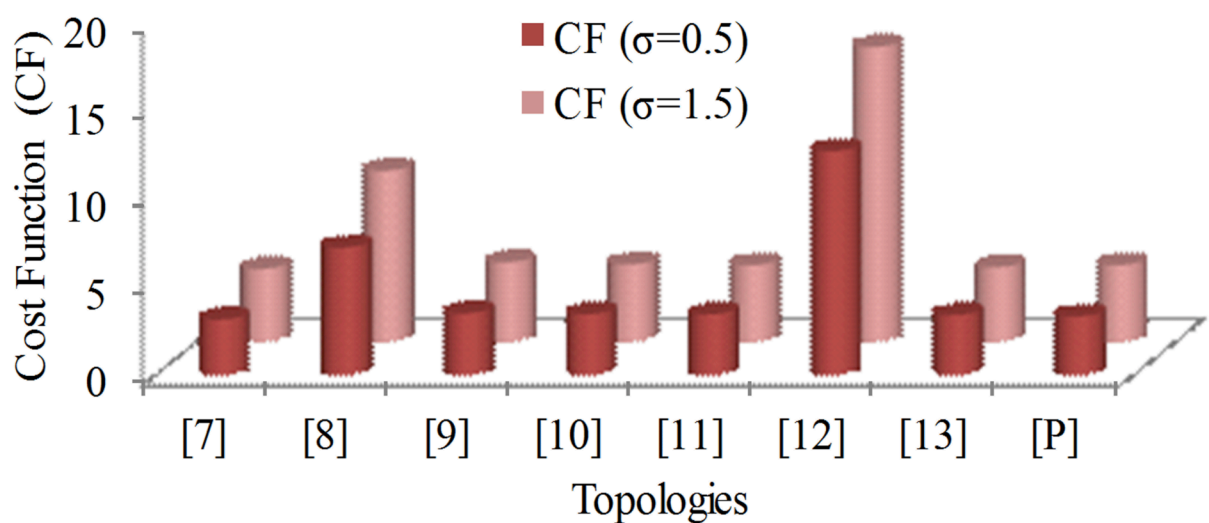
where σ is a constant and it represents the weight percentage of TSV [13,15,16,18]. Here CF is tested for $\sigma = 0.5$ and 1.5 . The presented architecture has a CF value comparable to that of the other listed topologies and has a much lower value than those of [14] and [18]. The MBV of the presented architecture and the topologies in [13] and [18] is six times the input DC voltage. The efficiency of the presented architecture is 95.71% at a 500W output power, higher than that of the study [13]. Further, efficiencies calculated in the research [14,15] and [19] will be reduced when the output power increases. The voltage gain of the presented architecture and the architectures in the study [13,15-17,19] is $6V_{DC}$, which is higher than that of the research [14] and [18]. Thus, in terms of lowering the total cost and the number of switches, the presented architecture provides significant benefits. Figure 9 portrays the comparison of the proposed topology with other reference topologies on the basis of component count, TSV_{pu} , and cost function.



(a)



(b)



(c)

FIGURE 9: Comparison of the (a) components count (b) TSVpu (c) cost function

Ref.	N_{SW}	N_{gd}	N_D	N_C		$(N_{SW} + N_D + N_C)/N_L$	TSV_{pu}	CF ($\sigma = 0.5$)	CF ($\sigma = 1.5$)	MBV	η (%)	THD (%)	VB
[13]	13	13	0	3		1.23	5.83	3.15	4.12	6	91.2@ 500W	NA	6
[14]	12	10	3	3		1.38	7.33	7.22	9.67	3	97.2@ 200W	4.9	3
[15]	14	13	1	3		1.38	6.0	3.5	4.5	4	97.4@ 200W	5.27	6
[16]	14	14	1	3		1.38	5.50	3.45	4.37	3	NA	NA	6
[17]	13	9	2	3		1.38	5.33	3.44	4.33	3	97.3@ 1kW	NA	6
[18]	12	12	0	4		1.23	6.0	12.67	16.67	NA	98.25 @1kW	5.3	1.5
[19]	11	6	3	4		1.38	4.83	3.4	4.21	6	97.3@ 400W	5.08	6
[P]	12	12	2	3		1.31	6.0	3.33	4.33	6	95.71 @500 W	5.35	6

TABLE 2: Comparison of the presented 13LSCMLI with similar 13 level single source topologies

N_{SW} , Number of switches; N_{gd} , Number of gate driver circuit; N_D , Number of diodes; N_C , Number of capacitors; TSV_{pu} , Total standing voltage per unit; MBV, Maximum Blocking Voltage; THD, Total Harmonic Distortion; VB, Voltage Boosting; NA, Not Available; CF, Cost Function; 13LSCMLI, 13-level switched-capacitor multilevel inverter

Simulation results

The feature set of the suggested 13LSCMLI architecture has been tested by electrical analysis utilizing MATLAB/SIMULINK and PLECS tools. To test the inverter's functionality, a 100V source is utilized. In order to compare the findings obtained from the simulation model, simulation factors are enumerated in Table 3. Using the NLC control approach, the simulation model tests the suggested architecture under varying resistive and inductive load circumstances. Figure 10(a-b) displays the simulated waveforms of the output voltage, output current, and capacitor voltages under dynamic load and varying

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modulation index conditions, respectively. Figure 10(a) displays the output voltage waveform at different load conditions, that is, $Z_1 = 100 \Omega$, $Z_2 = 100 \Omega + 120 \text{ mH}$, and $Z_3 = 50 \Omega + 120 \text{ mH}$, and the output voltage waveform exhibits 13 distinct levels, with the peak output voltage attaining about six times the input voltage, thus confirming the 13-level output and six times boost capability of the presented design. The capacitor's voltage ripple stays within an acceptable range of 10% of its maximum value. Figure 10(a) shows that the proposed inverter has a smooth transient response that does not affect its functioning. The waveform demonstrates that the proposed inverter performs admirably in all operational conditions, remains stable even when the load varies, and achieves effective capacitor voltage self-balancing. Figure 10(b) illustrates the variation in the number of output voltage levels corresponding to changes in the modulation index (MI). It is evident from Figure 10(b), as the MI alters from 1.0 to 0.8 to 0.6, the number of output voltage levels alters from 13 to 11 to 9, and the maximum voltage alters from $6V_{DC}$ to $5V_{DC}$ to $4V_{DC}$, respectively. From Figure 10(a) and (b), it is observed that the capacitor voltages are fairly distributed at their respective values with a slight reduction due to the internal resistance of the switching devices and the impedance of the conduction path, with a ripple voltage of less than 10% under varying MI conditions.

Figure 11 illustrates the voltage stress for all 12 switches with a load parameter of $100 \Omega + 120 \text{ mH}$. Switches S_1 to S_4 have a voltage stress equal to V_{DC} , S_5 and S_6 a voltage stress of $6V_{DC}$ while S_7 to S_{12} have voltage stress equal to $3V_{DC}$.

The FFT tool in the SIMULINK/Powergui block is used to perform harmonic analysis using 50 Hz as the fundamental frequency. The harmonic spectrum of the 13-level output voltage, with a %THD value of 5.35%, is displayed in Figure 12.

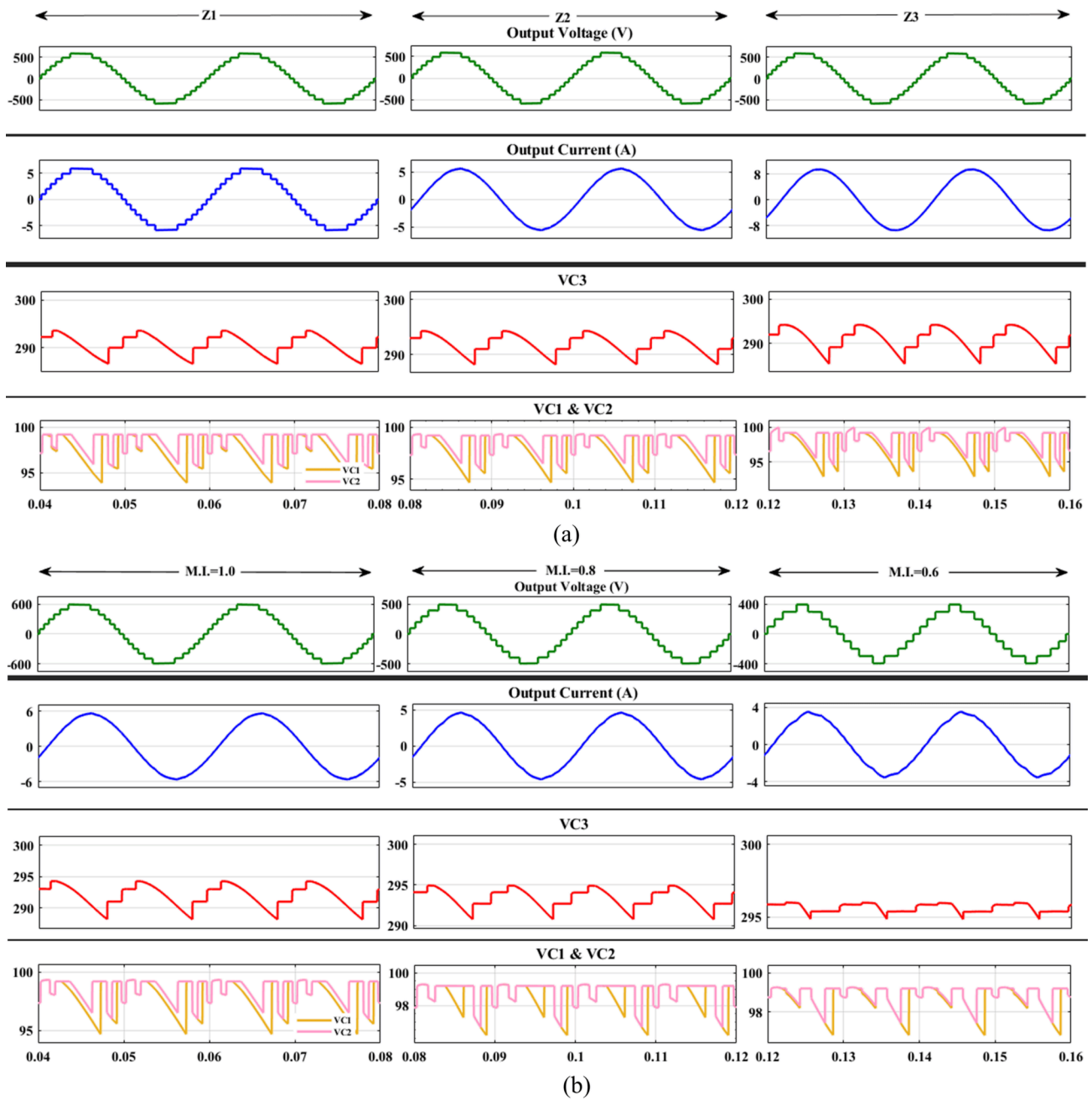


FIGURE 10: Simulation results of output voltage, output current and capacitor voltages with (a) dynamic load change (b) varying modulation index

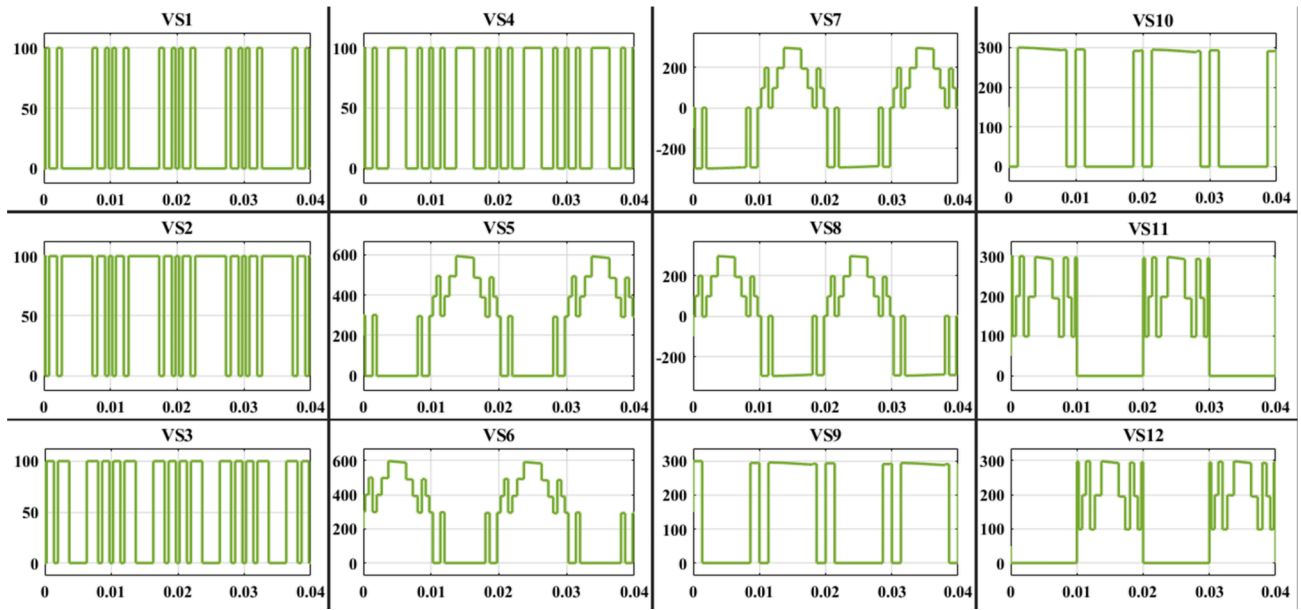


FIGURE 11: Simulation results of voltage stress of different switches

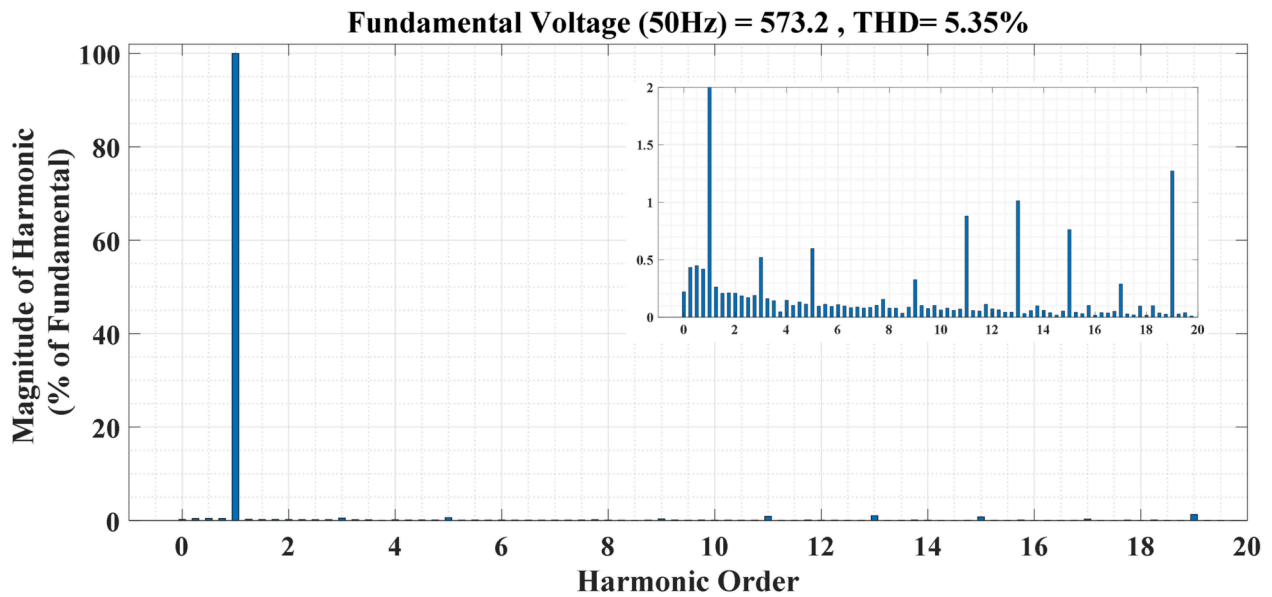


FIGURE 12: Harmonic spectrum of output voltage

THD, Total Harmonic Distortion

Experimental results

The proposed topology is experimentally verified. The components used and their specifications are displayed in Table 3. The output voltage and current waveforms for a dynamic load change are shown in Figure 13(a). It can be observed that the output waveform is stable after the load change. The output waveform when the MI is changed from 1.0 to 0.8 to 0.6 is shown in Figure 13(b). The number of voltage levels changes from 13 to 11 to 9 when the MI changes from 1.0 to 0.8 to 0.6

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0.6, respectively. The output voltage and current waveforms for a resistive load of $50\ \Omega$ are shown in Figure 13(c). Based on the applied DC voltage of 100 V, the peak output voltage is almost 600 V, confirming a sextuple voltage boost. The output voltage and current waveforms for an inductive load of $R = 50\ \Omega$, $L = 120\ \text{mH}$ are shown in Figure 13(d). As shown in Figure 13(d), the current waveform is sinusoidal in nature and lags the voltage waveform as expected.

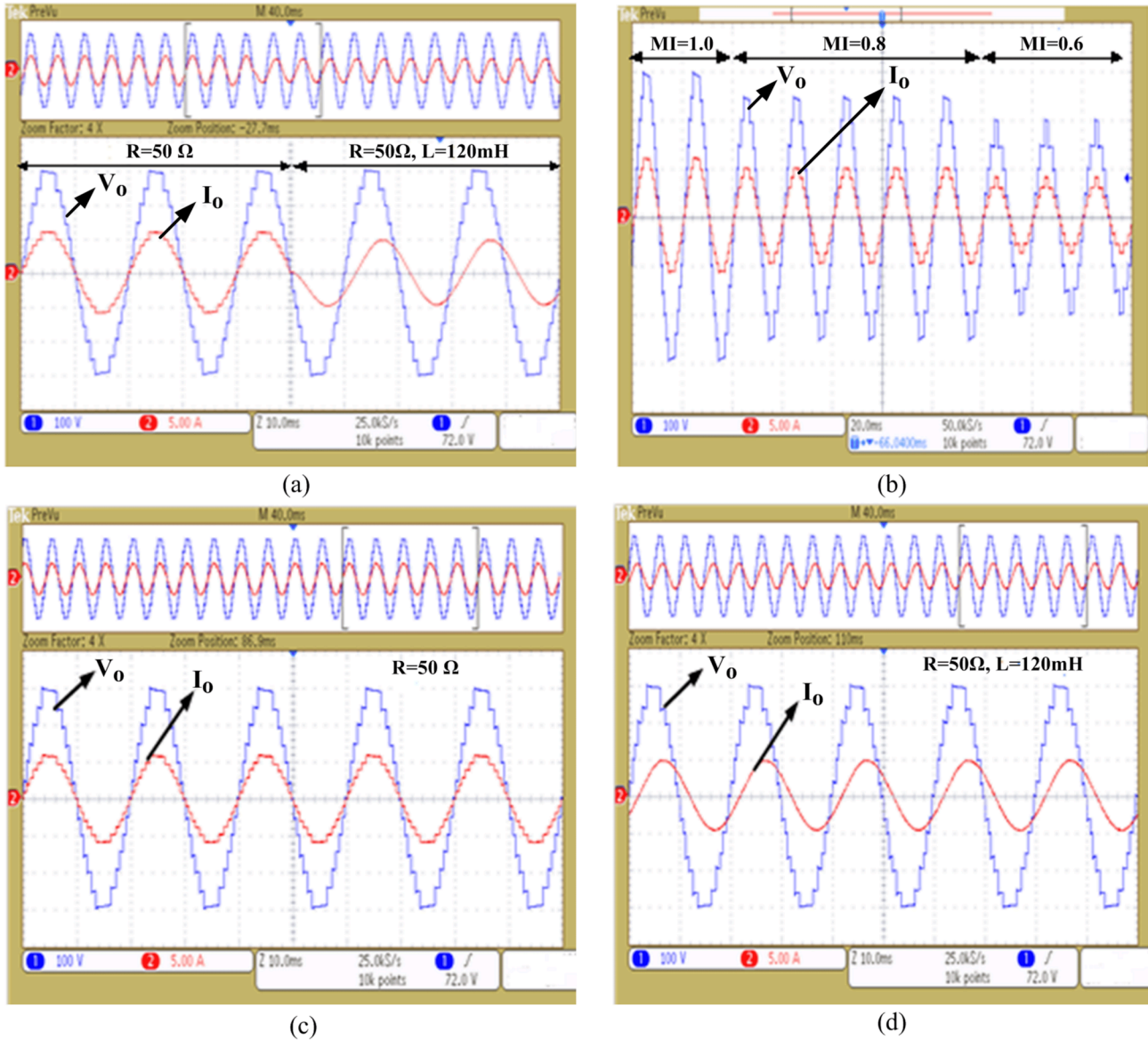


FIGURE 13: Experimental results: voltage and current waveforms for (a) dynamic load change (b) varying modulation index (c) R load (d) R-L load

Components	Simulation Values	Experimental Values
DC Voltage Source	100 V	100 V
Capacitors	1180 μ F, 762 μ F 100 V and 1371 μ F, 300 V	2200 μ F, 300 V
Load Resistance	50 Ω , 100 Ω	50 Ω
Load Inductance	120 mH	120 mH
Output Frequency	50 Hz	50 Hz
Switching Frequency	50 Hz	50 Hz
Driver	---	(TLP-250) 10-35 V/ $\pm$ 1.5 A
Controller	---	TMS320F28379D

TABLE 3: Simulation and experimental factors

Conclusions

A 13-level sextuple boost inverter with self-voltage balancing capacitors and reduced switch stress is presented in this study. The presented 13LSCMLI only needs 1 DC source, 3 capacitors, 12 switches, and 2 diodes to provide the necessary single-phase, 13-level ac output voltage with a sextuple voltage gain. Further, the maximum voltage stress across the switches is limited to six times the input voltage. The proposed architecture able to limit the voltage THD to 5.35% which is acceptable under IEEE standards. The suggested architecture offers a minimal component count with good efficiency, reducing system complexity and cost. The advantages of the presented 13LSCMLI architecture are proved through a detailed comparison with other existing topologies. Results from a comprehensive evaluation reveal that this design achieves a high efficiency of 95.71% at 500 W output power while utilizing fewer power switches, diodes, and capacitors to provide the same output voltage level as identical topologies in the literature. The NLC technique is utilized to generate the necessary switching pulses, and the outcomes are assessed using the MATLAB/Simulink platform. The effects of changes in MI and variations in the load are studied by analyzing the current and voltage waveforms at the output, and it is shown that the system remains stable throughout a wide variety of operating conditions. The experimental results validate the topology's feasibility and reliability under different circumstances.

Additional opportunities exist in this area since MLI topologies aim to reduce the number of components used in the inverter circuit. Since semiconductor components are the most common source of power electronics system failures, fault detection approaches may be easily extended in the near future with little hardware and computing requirements.

Additional Information

Author Contributions

All authors have reviewed the final version to be published and agreed to be accountable for all aspects of the work.

Concept and design: Mohammad Tufail

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Acquisition, analysis, or interpretation of data: Mohammad Tufail, Mirza Mohammad Shadab, Adil Sarwar

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Critical review of the manuscript for important intellectual content: Mohammad Tufail, Mirza Mohammad Shadab, Adil Sarwar

Supervision: Mirza Mohammad Shadab, Adil Sarwar

Disclosures

Human subjects: All authors have confirmed that this study did not involve human participants or tissue.

Animal subjects: All authors have confirmed that this study did not involve animal subjects or tissue.

Conflicts of interest: In compliance with [the ICMJE uniform disclosure form](#), all authors declare the following:

- **Payment/services info:** All authors have declared that no financial support was received from any organization for the submitted work.
- **Financial relationships:** All authors have declared that they have no financial relationships at present or within the previous three years with any organizations that might have an interest in the submitted work.
- **Other relationships:** All authors have declared that there are no other relationships or activities that could appear to have influenced the submitted work.

Data Availability Statements

The datasets (and/or code) supporting this study are available from the corresponding author upon reasonable request. All data generated or analyzed during this study are included in this published article and/or its appendices. Data sharing is not applicable. This work is theoretical; no datasets were generated or analyzed.

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