Cureus Journal of Engineering

Open Access Original Article

# Highly Efficient Fin type Field Effect Transistor (FinFET)-Based Analog to Digital Convertor Design for High-Speed Digital Electronics Applications

**Received** 06/19/2025
**Review began** 06/26/2025
**Review ended** 07/31/2025
**Published** 08/11/2025



**DOI:**
https://doi.org/10.7759/s44388-025-07886-3

Mahadevi S. Manur [1] , Kiran Bailey [2]

1. Electronics and Comunication, Don Bosco Institute of Technology, Bengaluru, IND 2. Electronics and Comunication, B.M.S. College of Engineering, Bengaluru, IND

**Corresponding author:** Mahadevi S. Manur, madhu@dbit.co.in

## Abstract

Analog Digital Converter (ADC) is the commonly used front-end device in most electronics in multi-domain applications. Because of this, ADC is more important than other components used in integrated applications. The conversion speed is one of the essential factors in the ADC because the further stages of the system should sync with the conversion speed of the ADC used. This work proposes a new circuit for ADC using Fin type Field Effect Transistor (FinFET) technology with fewer nodes. The comparator used a differential amplifier with a buffer circuit to reduce the power consumption and area requirements. Differential voltage calculation modules in the comparator are performed using four FET devices, and an inverter circuit is used to perform the inversion operation performed by the comparator. The buffer circuit produces the smooth output obtained from the comparator module. 12-bit ADC is designed and tested with linear and alternative wave signals to evaluate the performance of the proposed circuit. 4096-12-bit priority encoder performs the encoding operation, which requires input from the comparator module and performs encoding. A pass transistor-based XOR gate is implemented to develop a 12-bit encoding operation. This work used a Predictive Technology Model 14 nm FinFET device to implement all internal modules' circuits. Speed, area, and power consumption are measured and compared to conventional ADC circuits to evaluate the performance. This work consumes 0.007 mV power with a supply voltage of 0.6 V. Our work consumes a sum of 0.0037 $mm^2$ area and power consumption of 0.005 mW with a supply voltage of 0.9 V.

**Categories:** Electronics Design and VLSI, Embedded Systems and IoT, Engineering Management
**Keywords:** analog to digital convertors (adc), finfet, differential amplifier, voltage comparator, 12-bit adc, priority encoder, predictive technology model, 14nm technology, data convertors

## Introduction

Many digital systems interact with their environments by detecting analog signals from such transducers since analog signals originate from various sources and sensors that may monitor sound, temperature, light, or movement in the actual world. The comparator is employed as a fundamental element or component in the bulk of the arithmetic aspects of digital structures. Comparators are used in numerous hardware apparatuses for various applications outside digital systems because of their efficient performance, compact design, and reasonable price. Therefore, they have a big role in many diverse parts and circuits [1].

These comparator components may be used singly when the comparison is the primary goal or integrated into different courses when the comparison is only a minor component of several applications. In controlling and inspecting operations, comparators are often used, and these analyses are carried out in line with the requirements. They are frequently employed in limit-setting equipment to determine a component's tolerance or the highest or lowest temperature it can withstand. The comparator is the fundamental component of many control systems. Comparators are also employed in the quality control of goods. Comparators are used in quantitative measurements made by devices like scales. Moreover, it is utilized in signal processing and picture processing. The transistors' dimensions have been downscaled due to Very Large Scale Integration [2].

In traditional below 20 nm technology, Metal Oxide Semiconductor Field Effect Transistors are observed. These problems were overcome with the development of the FinFET transistor (Fin type Field Effect Transistor). The gate wraps around the channel in this three-dimensional, non-planar device. More control over the short channel effects is possible because of multi-gate coupling to the channel. These are the lower technological nodes' most promising gadgets. With a FinFET, the silicon wafer serving as the transistor's substrate is wrapped around the conducting channel [3].

**How to cite this article**
Manur M S, Bailey K (August 11, 2025) Highly Efficient Fin type Field Effect Transistor (FinFET)-Based Analog to Digital Convertor Design for High-Speed Digital Electronics Applications. Cureus J Eng 2 : es44388-025-07886-3. DOI https://doi.org/10.7759/s44388-025-07886-3

The thickness of the device affects the channel length. Typically, it has two gates. Either silicon wafers or SoI are the foundations for this double-gate transistor. The type of FinFET depends on the base on which it is manufactured. FinFET uses many gates to block or limit off-state leakage current while allowing sufficient current in the driving or ON state. Moreover, these several gates aid in electrically regulating the channel. There has recently been a rise in the demand for low-power devices like wearable and portables to sense biological signals. Biopotential signals range in frequency from 0 to 10 KHz and are typically feeble. An Analog Digital Converter (ADC) comes after an instrument front-end amplifier and filter in a typical biomedical system [4].

The digital signal processor is then given the digital output. Due to noise shaping and oversampling properties, Sigma delta ADCs are predominantly suited for high-resolution and low-frequency applications. In essence, there are two different modulator topologies depending on the type of filter circuit. These include an R1C1 filter, a 1-bit quantizer in the forward path, and a 1-bit DAC acting as an inverter beneath the feedback path. The modulator's power dissipation is reduced using passive integrators and low-power comparators [5].

The paper is organized as follows. First, detailed information about the previous circuits used for the ADC process is explained. Next, detailed information about the proposed ADC architecture is provided with a mathematical description. Then, the circuit analysis and performance measures compared with previous techniques are discussed with quantitative results. Finally, the paper concludes with a detailed summary of this work.

# Materials And Methods

## Literature survey

Chandra et al. proposed that, proportional to traditional designs, there is a relative drop in the overall number of switching devices utilized, which probably resulted in a drop in the number of transistors required. The suggested approach also does away with the need for additional inverters. The 2:1 multiplexer is used to first translate the input thermometer code into the appropriate gray code. After that, the gray code is converted to the appropriate binary code using two-input XOR gates. Results from the simulation show that the power consumption is down by around 80%, which is a significant reduction when compared to the encoder designs that are now in use and those that were previously known. The latency is also down to 0.366 ps. This sheds light on contemporary power-saving encoder designs and is more important in the long run. The suggested encoder provides better applicability for upcoming improved ADC generations and associated circuitry [6].

Sreenivasulu and Vadthiya proposed studying the impact on n-channel SOI JL vertically stacked (VS) nanowire (NW) FETs at 10 nm gate length (LG) of symmetric and asymmetric spacer length adjustments toward source and drain. Along with the dimensions of the device's width, height, and aspect ratio (AR), spacer length has been shown to be one of the most important performance parameters. The symmetric spacer length (LSD), source side pacer length (LS), and drain side spacer length (LD) are the physical variations in this study. In contrast to LS and LSD, which have comparable effects on ION/IOFF ratio, the simulation findings show that the LD variant has the greatest ION/IOFF ratio. The device ensures low power and great switching drivability at 25 nm and provides substantial ON current with the maximum ION/IOFF ratio and optimal subthreshold slope (SS) [7]. Sarada suggested using two new concurrent error repairable carry select adders (CSLAs). The suggested concurrent error repairable CSLA finds and fixes the circuit's defects. CSLA II is suggested to provide the precise position of the fault. The concurrent error repairable CSLA II that has been presented provides the bit location of the fault in addition to fault detection and repair. Compared to the CSLA I that is suggested, it requires less time, space, and power. Using the NCLaunch tool, the proposed concurrent error repairable CSLAs are simulated. The results of the simulations demonstrate the complete error recovery of the suggested designs [8]. James et al. proposed an SB-DFE, or sliding-block decision feedback equalizer, that solves the enactment difficulties of traditional DFEs without sacrificing presentation. A nine-tap system is confirmed using a 112-Gb/s ADC-digital signal processor (DSP) four-level pulse amplitude (modulation LR wireline receiver built in a 7-nm FinFET). The design breaks the DFE's feedback loop and enables logic pipelining by dividing the incoming signal into overlapping but computationally independent pieces. The computational cost of the SB-DFE may be arbitrarily modest for any tap/count, in contrast to previous feedback-breaking approaches; in fact, it demonstrates the viability of SB-DFE implementations with more than 30 taps [9].

Gain et al. proposed that discrete multitone (DMT) modulation is used in the wireline receiver (RX) data path while communicating across electrical networks. A synthesized, autonomously inserted, and routed DSP follows a 10-bit time-interleaved pipelined successive-approximation register ADC in the DMT RX's entirely digital equalization data path (TI-PISAR ADC). The 14-nm FinFET prototype RX device exhibits a 56 Gb/s lane data throughput while dissipating 161 mW total, comprising the power from the ADC and DSP. While collaborating over channels that had up to 28 dB of loss at 14 GHz and a bit-error-rate (BER) greater than 2e-4, the energy efficiency of the DSP was 1.2 pJ/b, and the total RX was 2.9 pJ/b [10].

Rajasekhar et al. proposed an approximate carry select adder with reverse carry propagation. The reverse carry propagate full adder (RCPFA) was used in the design of this RCSLA. The carry input is more significant than the carry output in the RCPFA structure because the carry signal propagates in the opposite direction, from the MSB component to the LSB part. On the basis of the design specifications, three different implementation types were created in RCPFA. To create different varieties of approximation adders, same methodology was applied to RCA and CSLA. These designs and simulations were carried out using the 45 nm COMS technology and the CADENCE software tool. The three RCPFA-based CSLA implementations' design parameters are contrasted with those of the current CSLA adders [11].

Saleh and Hamed proposed that the nonlinear X-shaped photonic crystal ring resonators (X-PCRRs) are the foundation of a novel optical analog-to-digital converter (OADC) architecture. X-PCRRs are created using silicon-based nonlinear rods and silicon-based dielectric rods. A nonlinear three-channel demultiplexer and an optical encoder make up the suggested configuration. The optical encoder produces two-bit binary codes based on the output channel number of the nonlinear demultiplexer, which transforms the continuous input signal into three quantized discrete levels. The photonic band structure and light propagation inside the Photonic Crystal (PhC)-based structure are studied and analyzed, respectively, using two well-known plane wave expansion and finite difference time domain techniques. The second window of communications in the C-band is covered by the broad TM photonic band gap of the basic PhC [12].

## Proposed method

Figure *1* shows the Block representation of the proposed ADC architecture. The significant components include offset voltage generation, offset addition, and reference voltage generation using ladder circuits: comparator, buffer circuit, and priority encoder. Initially, the input will be preprocessed by adding a reference offset voltage to improve the voltage conversion accuracy. The offset voltage deviation is used to normalize the input signal for the convertible region. The offset added the analog signal feed to the comparator stage to generate differential output. The comparator has a differential calculation unit and buffer inverter to generate the differential voltage output. The buffer circuit generates the accurate comparator output for digital conversion. For a 12-bit ADC, 256 single comparators are required to generate the 256 values fed through the priority encoder. The decimal representation of the input signal is generated in the priority encoder for storage or further processing.

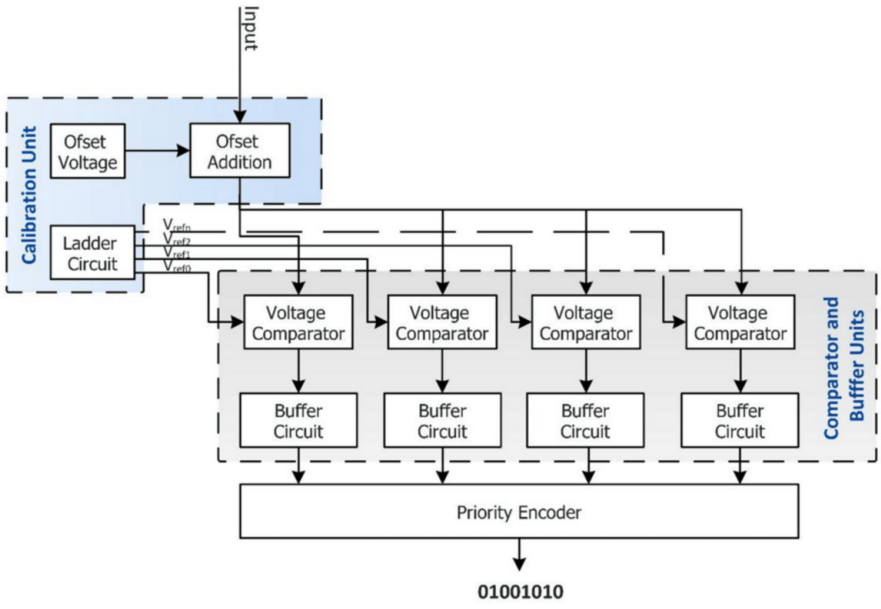


**FIGURE 1: Block representation of proposed ADC architecture**

ADC, Analog Digital Converter

The mathematical equations of proposed ADC architecture for computing the static and dynamic performance parameters are as given. The static performance parameters include differential nonlinearity (DNL) and integral nonlinearity (INL). The dynamic performance parameters are Signal to Noise Ratio (SNR), Signal to Noise ratio and distortion, total harmonic distortion, and Effective number of bits.

If we consider Δ(delta), as small deviation with Vref as the reference voltage and N as the number of bits resolution for flash ADC. The deviation is defined as $\Delta = Vref / 2^N$. Differential nonlinearity is computed by $DNL(i) = vin(i) - vin( i -1)/\Delta$ and $INL(i) = {}_{i=1}^{K}\sum DNL(K)$.

The dynamic performance parameters, SNR is computed by, SNR = Signal Power/Noise Power and ENOB = (SNR - 1.76)/6.02

$SNR = (Vref^2 / 8)/(\Delta^2 / 12)$

$10\log_{10}SNR = 6.02N + 1.76$ DB

### *Comparator Unit*

A comparator is a significant unit in the analog-to-digital conversion process. Generally, a differential voltage calculation circuit will be used to perform the comparator operation [11,12]. A voltage input (VIN) signal is functional to one input of the comparator, while orientation voltage (VREF) is to the other [13]. The comparator's digital logic output state, which can be either a "1" or a "0," is determined by comparing the two voltage levels at its input. After scheming an N-bit flash ADC, 2N - 1 comparators are required. The power and space consumed per comparator are crucial for medium-resolution ADCs. Hence, power and area consumption must be constant while comparing various comparator topologies for usage in a flash ADC. Imagine that a single-stage amplifier and a two-stage amplifier are being compared [14-19]. The single-stage amplifier employs area A and draws I current. The two-stage amplifier draws $I_1 + I_2$, current and uses $A_1 + A_2$, the area where the 1 and 2 subscripts elect the first and second phase, correspondingly. $I_1 + I_2 = I$ and $A_1 + A_2 = A$ .

The channel length L is expected to be kept to a least and the device width W controls the area.

$$W_1 + W_2 = W$$

When the existing in phase one of the two-stage amplifier grows, the frequency width necessity likewise intensifies to maintain constant node voltages. Thus

$$\frac{I_1}{W_1} = \frac{I_2}{W_2}$$

The transconductance is given by $g_m = \sqrt{2\mu C\left(\frac{W}{L}\right)}$

Therefore

$$(g_{m1} + g_{m2})^2 = \frac{2\mu C_{OX}}{L}(W_1 I_1 + W_2 I_2 + 2)\sqrt{W_1 I_1 W_2 I_2}$$

$$= \frac{2\mu C_{OX}}{L}(W_1 I_1 + W_2 I_2 + W_1 I_2 + W_2 I_1)$$

$$= \frac{2\mu C_{OX}}{L(W_1 + W_2)} I_1 + (I_1 + I_2) W_2$$

Thus

$$(g_{m1} + g_{m2})^2 = G_{m2}$$

A linear amplifier may come before it to ensure the voltage supplied to the dynamic latch is high enough to counteract this offset. The ability to offset-cancel a linear amplifier makes medium-resolution (8-bit) converters viable. The offset-cancellation switch S1 connects to ground. The offset-cancellation amplifier ( 2) forces its offset ($Vos_2$) and the offset ($Vos_l$) from the high-gain amplifier $g_{m1}$ onto the offset-cancellation capacitors $C_{ocl}$ and $C_{oc2}$.

$$V_{\text{off}} = \frac{g_{m1} V_{\text{os1}} + g_{m2} V_{\text{os2}}}{(1 + g_{m2}) R_L}$$

Input-referred offset voltage $V_{os}$ is condensed by the voltage by

$$V_{os} = \frac{g_{m1}V_{os1} + g_{m2}V_{os2}}{g_{m1}R_L(1 + g_{m2}R_L)^2}$$

The amplify cycle initiates by flinging the switch to activate the switch and measure the input voltage. At present, the amplifier output voltage is a growing exponential whose concluding value is the product of the input voltage and the voltage gain. Once the voltage is large sufficient (approximately 50 mV), the active latch is empowered. Because of its positive feedback, it may quickly "amplify" the pass voltage to values close to logic levels. The result is then held until the encode logic is activated by activating the storage latch. Figure 2 shows the proposed comparator implemented using a 14 nm FET device with an output buffer.

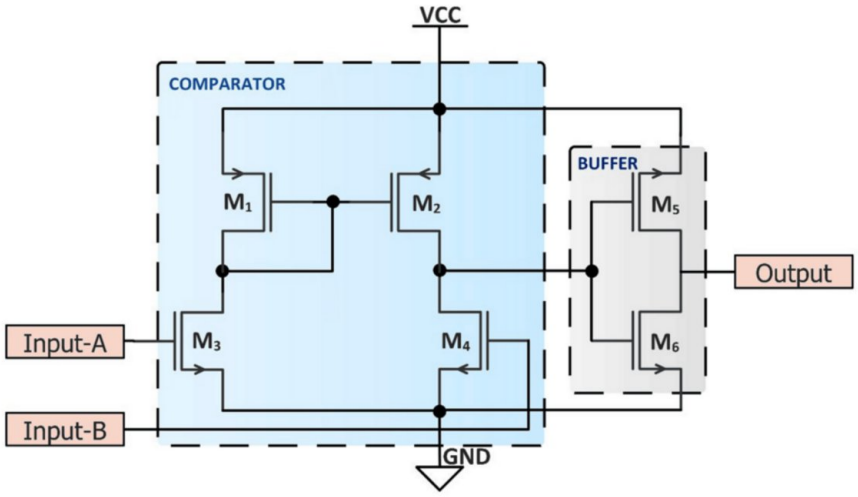


**FIGURE 2: Proposed comparator using FET device with output buffer**

FET, Field Effect Transistor

Figure 3 shows the output obtained for different reference voltages, Vref. An exponential voltage source is used to test the proposed comparator. The range of the testing signal is varied from 0 to 0.9 V. To analyze the characteristics, the reference voltage varies from 0.2 to 0.8 with an increment of 0.1 V. The dotted lines in Figure 3 show the different reference voltage input. The figure shows that the output voltage is correctly generated concerning other reference voltage inputs. The Figure 4 shows the output graph of 32-bit comparator array and the Figure 5 shows the schematic of cascaded 8-bit comparator as below.

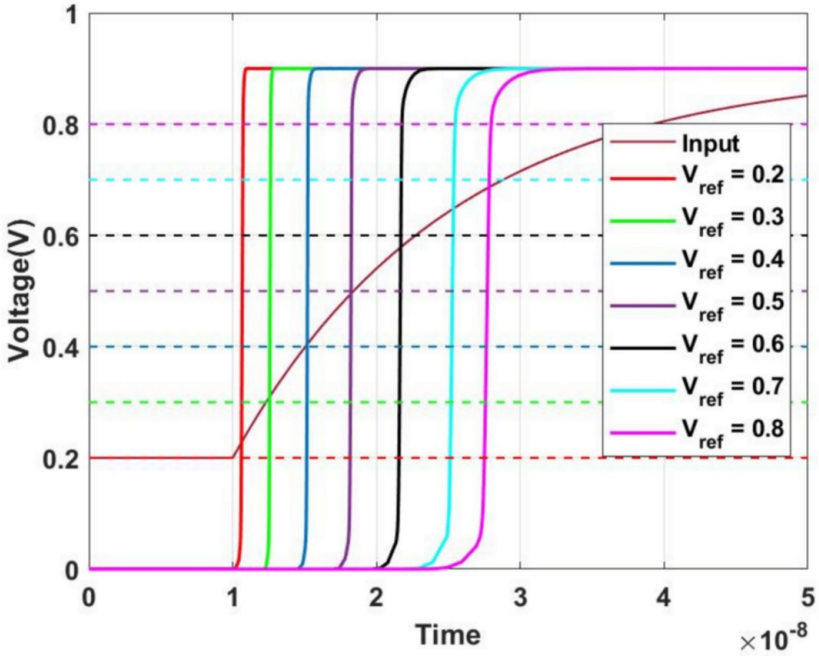


**FIGURE 3: Proposed comparator output with a different reference voltage**

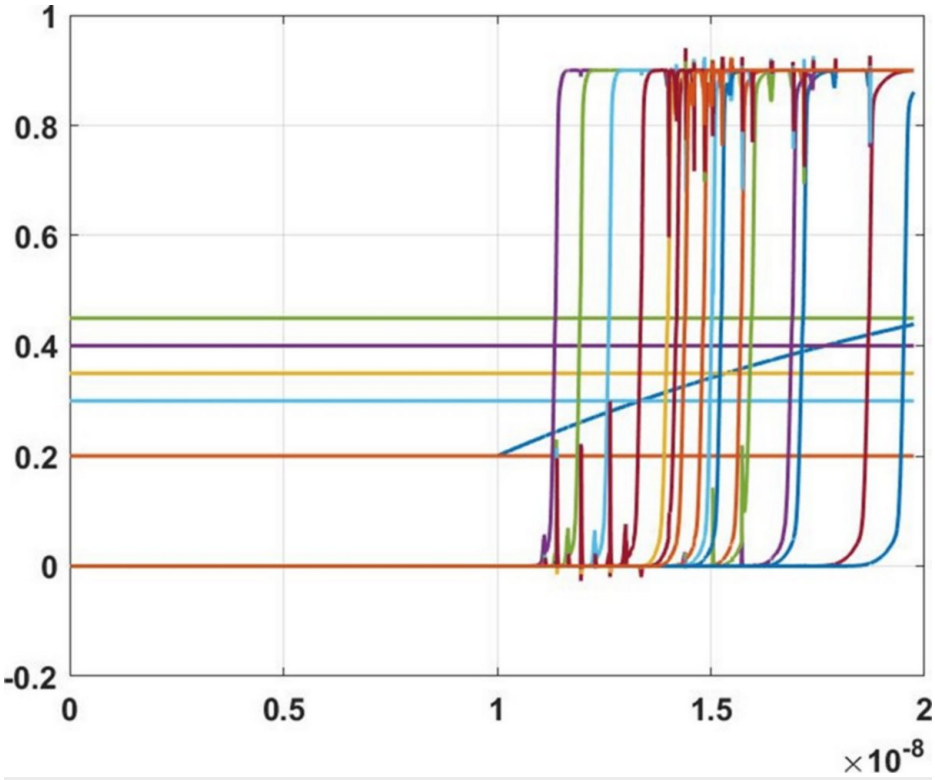


**FIGURE 4: The 32-comparator output for ADC module**

ADC, Analog Digital Converter

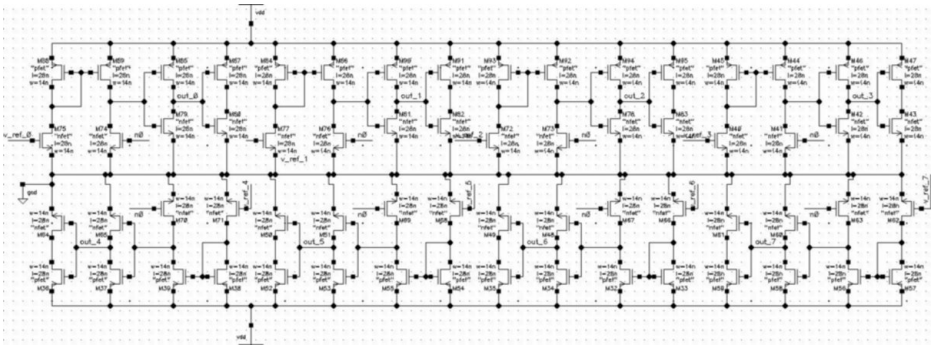

**FIGURE 5: The 8-bit comparator array**

### *8 to 3 Priority Encoder*

Eight inputs and three outputs make up this kind of encoder [20-25]. The input with the greatest priority is thought to reflect the output when numerous inputs are active high simultaneously. This encoder has several characteristics, such as the cascade of n bits for priority encoding [26-28], encoding of inputs with the greatest priority [29,30], code conversions [31], converting decimal to BCD [32-34], and enabling an output line with an active low when all the input lines are active high. Figure *6* shows the transistor-based XOR gate is used in the priority encoder to perform decimal encoding.

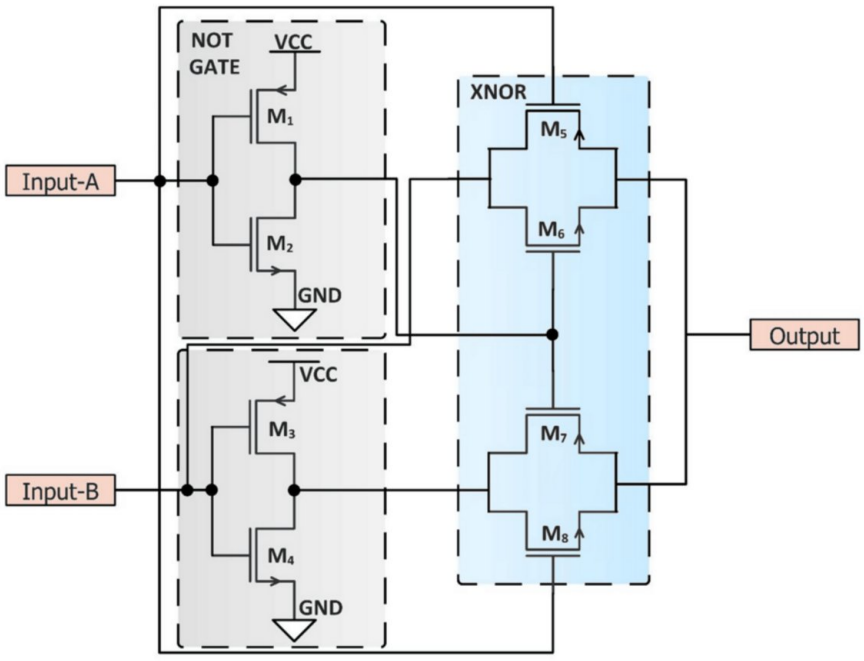


**FIGURE 6: Pass transistor-based XOR gate used in the priority encoder of the ADC**

ADC, Analog Digital Converter

To implement the XOR gate, 14 nm FinFET is used with the pass transistor logic technique. The inputs A and B are first inverted using conventional NOT gates implemented using FinFET. The XNOR operation uses 4 FinFET devices. The waveform obtained for the pass transistor-based XOR gate with different input combinations are shown in Figure *7*.

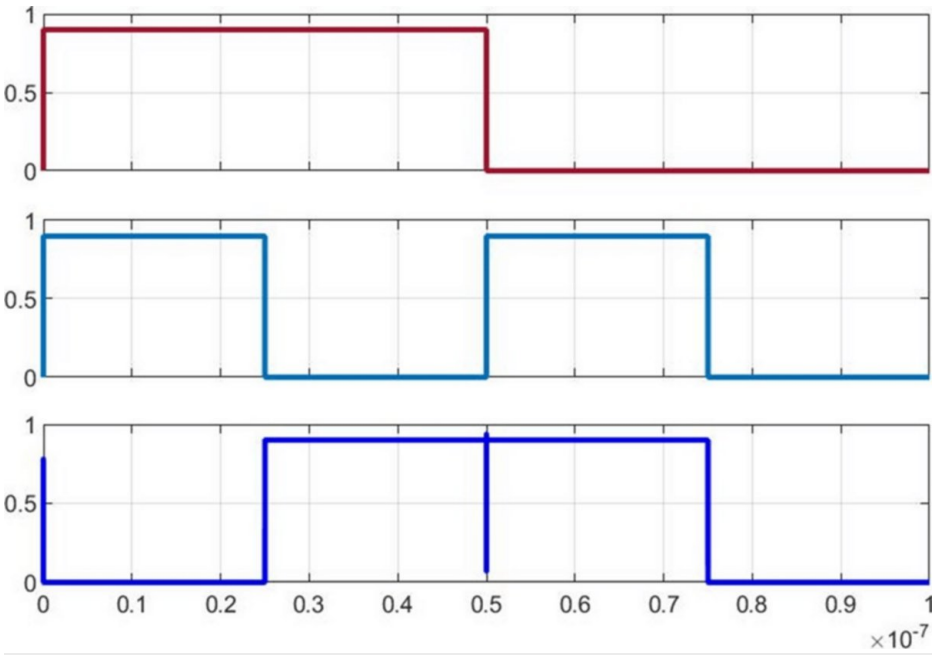


**FIGURE 7: Pass transistor-based XOR gate output waveform**

The complete implementation of the priority encoder used to perform the decimal encoding process can be shown in Figure *8*. To perform 256 to 8-bit encoding, eight 128-bit EXOR gates are required. For the first XOR gate, the last 128 comparator outputs are considered the input.

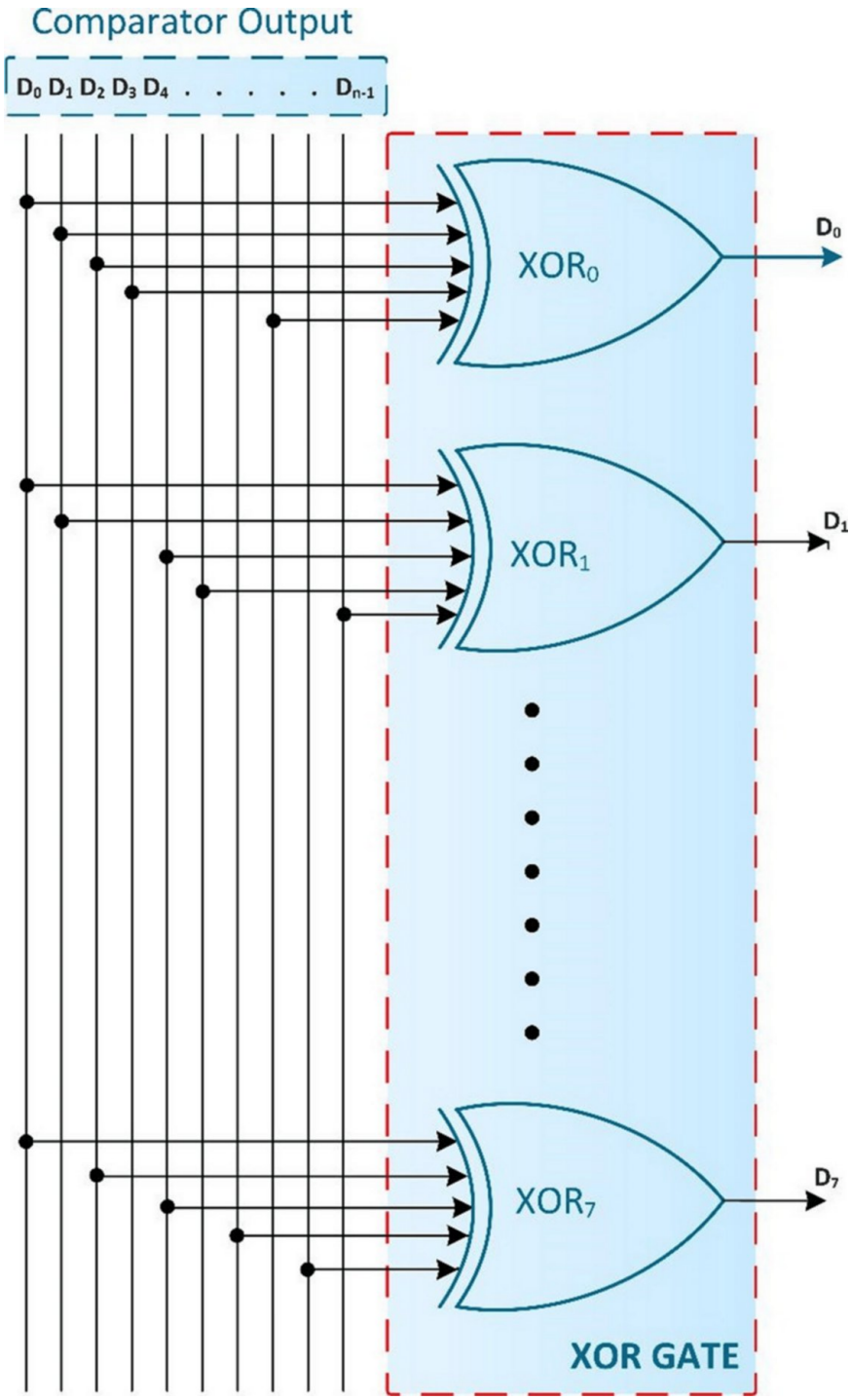


**FIGURE 8: Priority encoder architecture for proposed ADC**

ADC, Analog Digital Converter

For the previous XOR gate, the intermediate comparator outputs are considered inputs. The comparator output obtained for 5-bit ADC is shown in Figure *9*. The red color plot shows the LSB, and the black color plot shows the MSB of the converted binary sequence.

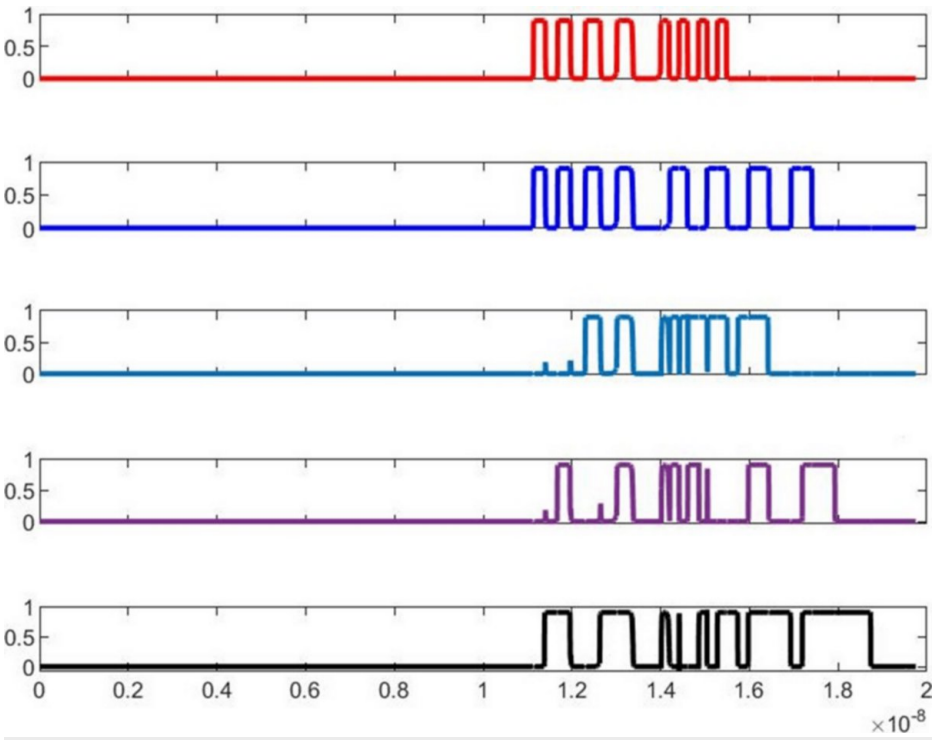


**FIGURE 9: Output produced from the priority encoder module**

## Results And Discussion

The proposed ADC implementation uses cadence virtuoso software in a Linux environment. PTM 14 nm FinFET library performs all the circuit implementations as a node. MATLAB software is used to perform the overall area calculation based on the number of FETs used in each module. ADE simulator in the cadence virtuoso module is used to perform each module's transient and DC analysis. The PTM 14 nm FinFET parameters and their values are displayed in Table *1*.

| S. No. | Parameters | Value |
|---|---|---|
| 1 | Channel Width | 14 nm |
| 2 | Channel Length | 20 nm |
| 3 | Gate Length | 14 nm |
| 4 | Supply Voltage | 900 mV |
| 5 | Minimum Current | 1e-008 |
| 6 | Maximum Current | 3e-008 |

**TABLE 1: PTM 14 nm FinFET parameters**

PTM, Predictive Technology Model; FinFET, Fin type Field Effect Transistor

Table *2* shows the performance of the proposed method based on bits. The table shows that the power consumption and area are directly proportional to the number of bits used. If the number of bits increases, the area and power consumption also increase linearly. For an 8-bit comparator, 28 FinFET devices are used and obtained an area of 0.0000188160 $mm^2$ with a power consumption of 1.35 mW. For fewer comparators, a higher voltage step should be used, which limits the conversion precision. The voltage step used for the 8-bit comparator is 150 mV. The 16-bit comparator consumed 56 FinFET with a power consumption of 2.19 mW and an area of 0.0000376320 $mm^2$. A maximum of 1016 FinFET with

0.0006021120 $mm^2$ area and 2.89 mW power is consumed for 256 comparators used for 8-bit ADC. The 512 comparator consumes 2029 of FET, 0.0007985459 $mm^2$ area, 3.25 mW power with a 4 mV voltage step of the 9-bit ADC. The 2698 of FET, 0.0008369841 $mm^2$ area, 3.96 mW of power are consumed for 10 bit. The 11-bit needs 3185 of FET, 0.0009876536 $mm^2$ area, and 4.58 mW power. The 12-bit consumes 3978 of FET, 0.0009987655 $mm^2$ area, 4.99 mW power for a 4096 comparator ADC.

| #Comparator | # FET | Area ($mm^2$) | Ref .voltage step | Power (mW) |
|---|---|---|---|---|
| 8 bit | 28 | 0.0000188160 | 150 m | 1.35 |
| 16 bit | 56 | 0.0000376320 | 100 m | 2.19 |
| 32 bit | 120 | 0.0000752640 | 50 m | 2.28 |
| 64 bit | 248 | 0.0001505280 | 25 m | 2.5 |
| 128 bit | 504 | 0.0003010560 | 12.5 m | 2.7 |
| 256 bit | 1016 | 0.0006021120 | 6 m | 2.89 |
| 512 bit | 2029 | 0.0007985459 | 4 m | 3.25 |
| 1024 bit | 2698 | 0.0008369841 | 3 m | 3.96 |
| 2048 bit | 3185 | 0.0009876536 | 1.5 m | 4.58 |
| 4096 bit | 3978 | 0.0009987655 | 1.1 m | 4.99 |

**TABLE 2: Number of FET devices for various bits of comparator**

FET, Field Effect Transistor

Table *3* shows the number of FET devices for the priority encoder. Encoding modules consume maximum resources and power when compared to the other modules.

A 3-bit encoder consumes 18900 FinFET devices and 5.17E-05 $mm^2$ area and a power consumption of 0.56 mW. A 4-bit encoder consumes 37856 FinFET devices and 0.00012 $mm^2$ area and power consumption of 0.82 mW.

An 8-bit encoder requires 256 comparator output, and it consumes 610240 FinFET devices and 0.00378 $mm^2$ area and a power consumption of 0.95 mW. Table *4* shows the overall number of FET, power consumption and area requirement for 8-bit ADC. Here the total area is the sum of the area consumed for the comparator and the priority encoder.

| Resolution | # FET | Area ($mm^2$) | Power (mW) |
|---|---|---|---|
| 3 bit | 18900 | 5.17E-05 | 0.56 |
| 4 bit | 37856 | 0.00012 | 0.82 |
| 5 bit | 75864 | 0.00031 | 0.86 |
| 6 bit | 152016 | 0.00073 | 0.91 |
| 7 bit | 304584 | 0.00168 | 0.93 |
| 8 bit | 610240 | 0.00378 | 0.95 |

**TABLE 3: Number of FET devices for encoder**

FET, Field Effect Transistor

Table 4 shows the overall number of FET, power consumption, and area requirement for 12-bit ADC. Here the total area is the sum of the area consumed for the comparator and the priority encoder. The 9-bit resolution needs 723697 of FET, 4 m of ref. voltage step, 0.00426 $mm^2$ area, 2.3 mW of power, 10-bit resolution requirements 793568 of FET, 3.2 m of ref. voltage step, 0.00536 $mm^2$ area, 2.9 mW of power, 11-bit resolution desires 836857 of FET, 2 m of ref. voltage step, 0.00657 $mm^2$ area, 3.3 mW of power, 12-bit resolution essentials 889741 of FET, 1 m of ref. voltage step, 0.00869 $mm^2$ area, 3.8 mW of power.

| Resolution | # FET | Ref. voltage step | Area ($mm^2$) | Power (mW) |
|---|---|---|---|---|
| 7 bit | 18900 | 150 m | 5.17E-05 | 1.35 |
| 8 bit | 37856 | 100 m | 0.00012 | 1.45 |
| 9 bit | 75864 | 50 m | 0.00031 | 1.6 |
| 10 bit | 152016 | 25 m | 0.00073 | 1.9 |
| 11 bit | 304584 | 12.5 m | 0.00168 | 2.05 |
| 12 bit | 610240 | 6 m | 0.00378 | 2.2 |

**TABLE 4: Overall number of FET, area, and power consumption of ADC**

FET, Field Effect Transistor; ADC, Analog Digital Converter

Table 5 shows the performance of the proposed method with previously implemented ADC architectures. Various technologies, such as 28LP, CMOS65 nm, and CMOS40 nm were used to implement ADC. Lower technology, such as CMOS 45 nm and CMOS 60 nm consumes higher area and power consumption when compared with recent technologies. Hyeonsik et al. proposed a new architecture for ADC circuit for high-speed conversion process. This is implemented using 28 nm low power FinFET technology based 9-bit flash ADC. The maximum supply voltage provided is 0.9 V and consumed a power consumption of 2.6 mV and area of 0.0525 $mm^2$. Minki et al. proposed a SAR ADC circuit with speed of 100MS/s with power consumption of 33 mV and area of 0.756 $mm^2$. This circuit uses 28 nm low-power FinFET technology to cover an input range of 440 mV with a maximum supply voltage of 0.9 V. A CMOS40 nm technology-based SAR ADC is proposed by Oration et al. with a conversion ratio of 2.8KS/s. This work consumes 0.007 mV power with supply voltage of 0.6 V. This circuit consumes a sum of 4.9 $mm^2$ area.

This work uses 14 nm FinFET technology with low power consumption and area. Our work consumes a sum of 0.0037 $mm^2$ area while other works consume area of 0.0525 $mm^2$, 0.756 $mm^2$, and 4.9 $mm^2$. Similarly, the proposed work consumes less power of 0.005 mW while other work consumes 2.6 mW, 33 mW, and 0.007 mW.

| | Hyeonsik et al. | Minki et al. | Orazio et al. | This work |
|---|---|---|---|---|
| Process | 28LP | CMOS65 nm | 40 nm | 14 nm FinFET |
| Architecture | Flash | SAR | SAR | Flash |
| Supply voltage (V) | 0.9 | 0.9 | 0.6 | 0.9 |
| Input range | 110 mV | 440 mV | Full scale | 700 mV |
| Resolution | 9 | 8 | 8 | 8 |
| Sample rate | 0.5GS/s | 100MS/s | 2.8KS/s | 0.5GS/s |
| #FET | - | 8190 | - | 9664 |
| Power (mW) | 2.6 | 33 | 0.007 | 0.005 |
| Area ($mm^2$) | 0.0525 | 0.756 | 4.9 | 0.0037 |

**TABLE 5: Performance of proposed method with previous techniques**

Figure *10* shows the area utilization for different resolutions of the comparator, encoder, and overall ADC. The blue color bar shows the area required to implement the comparator circuit. The orange color shows the area required to implement the encoder. The gray color shows the overall area consumed by the ADC circuit.

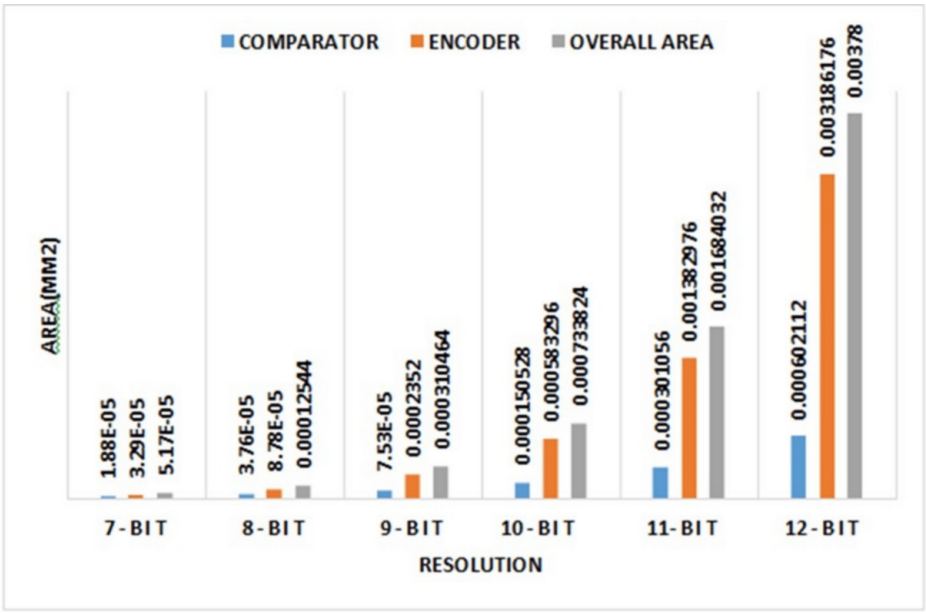


**FIGURE 10: Area utilization for different bit sized ADC**

ADC, Analog Digital Converter

Figure *11* shows the comparison of the area required for the previous implantation with the proposed ADC circuit.

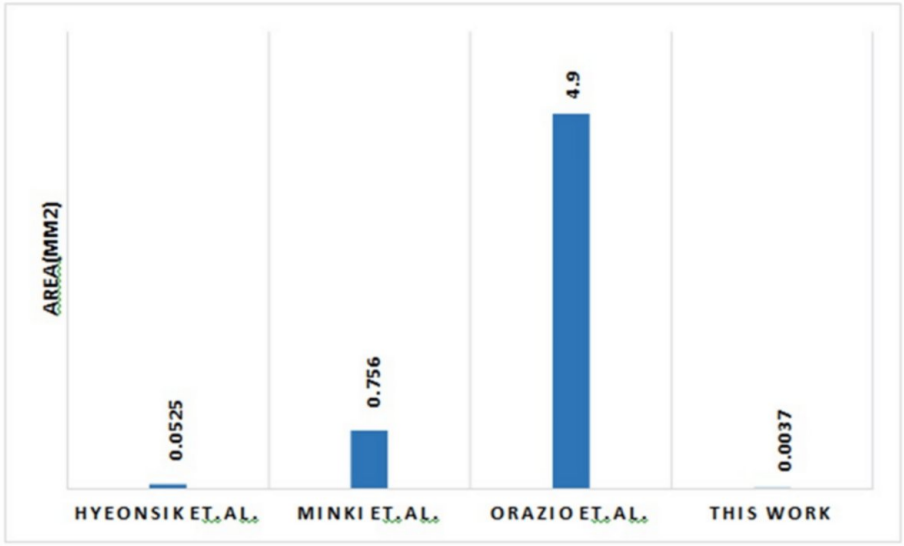


**FIGURE 11: Area comparison with other techniques**

## Conclusions

This work proposes a new simplified circuit to perform the analog-to-digital conversion process. The 14 nm FinFET device is used as a node to perform the circuit-level implementation of every module. Here comparator module is implemented using only four FinFET devices followed by a buffer circuit to make a smooth comparator output.

The proposed circuit is tested using exponential and sinusoidal signals to analyze the characteristics. Various evaluation metrics such as the number of FET devices, area, overall power consumption, and operating speed are evaluated to compare with the conventional conversion circuits.

The overall area and power consumption is reduced compared to traditional analog-to-digital conversion circuits. This work consumes a sum of 0.0037 $mm^2$ area while other works consume an area of 0.0525 $mm^2$, 0.756 $mm^2$, and 4.9 $mm^2$. Similarly, the proposed work consumes less power of 0.005 mW while others consume 2.6 mW, 33 mW, and 0.007 mW.

## Additional Information

### Author Contributions

All authors have reviewed the final version to be published and agreed to be accountable for all aspects of the work.

**Concept and design:** Mahadevi S. Manur, Kiran Bailey

**Acquisition, analysis, or interpretation of data:** Mahadevi S. Manur, Kiran Bailey

**Drafting of the manuscript:** Mahadevi S. Manur, Kiran Bailey

**Critical review of the manuscript for important intellectual content:** Mahadevi S. Manur, Kiran Bailey

**Supervision:** Kiran Bailey

### Disclosures

**Human subjects:** All authors have confirmed that this study did not involve human participants or tissue. **Animal subjects:** All authors have confirmed that this study did not involve animal subjects or tissue. **Conflicts of interest:** In compliance with the ICMJE uniform disclosure form, all authors declare the following: **Payment/services info:** All authors have declared that no financial support was received from any organization for the submitted work. **Financial relationships:** All authors have declared that they have no financial relationships at present or within the previous three years with any organizations that might have an interest in the submitted work. **Other relationships:** All authors have declared that there

are no other relationships or activities that could appear to have influenced the submitted work.

## Acknowledgements

We would like to thank Don Bosco Institute of Technology, Bengaluru, and B.M.S. College of Engineering, Bengaluru, for encouraging the work to be completed successfully.

## References

1. Senthilkumar VM, Ravindrakumar S, Nithya D, Kousik NV: A vedic mathematics based processor core for discrete wavelet transform using FinFET and CNTFET technology for biomedical signal processing. Microprocessors and Microsystems. 2019, 71:102875.
2. Hudner J, Carey D, Casey R, et al.: A 112Gb/s PAM4 wireline receiver using a 64-way time-interleaved SAR ADC in 16nm FinFET. 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA. IEEE, 2018. 47-48. 10.1109/VLSIC.2018.8502436
3. Zandieh A, Schvan P, Voinigescu SP: A 2x-oversampling, 128-GS/s 5-bit flash ADC for 64-GBaud applications. 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), San Diego, CA, USA. IEEE, 2018. 52-55. 10.1109/BCICTS.2018.8550990
4. Han J, Chang E, Bailey S, et al.: A generated 7GS/s 8b time-interleaved SAR ADC with 38.2 dB SNDR at Nyquist in 16nm CMOS FinFET. 2019 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA. IEEE, 2019. 1-4. 10.1109/CICC.2019.8780169
5. Jeon MK, Yoo WJ, Kim CG, Yoo C: A stochastic flash analog-to-digital converter linearized by reference swapping. IEEE Access. 2017, 5:23046-3051. 10.1109/access.2017.2766671
6. Pittala CS, Parameswaran V, Srikanth M, et al.: Realisation and comparative analysis of thermometer code based 4-bit encoder using 18 nm FinFET technology for analog to digital converters. Soft Computing and Signal Processing. Advances in Intelligent Systems and Computing. Reddy VS, Prasad VK, Wang J, Reddy KTV (ed): Springer, Singapore; 2021. 1:557-66.
7. Sreenivasulu VB, Narendar V: Circuit analysis and optimization of GAA nanowire FET towards low power and high switching. Silicon. 2022, 14:10401-411. 10.1007/s12633-022-01777-6
8. Musala S, Neelam AK, Sreenivasulu B, Vardhan KV: Concurrent error detectable and self-repairable carry select adder. International Journal of Electronics. 2021, 109:1954-972. 10.1080/00207217.2021.2001862
9. Bailey J, Shakiba H, Nir E, et al.: A 112-Gb/s PAM-4 low-power nine-tap sliding-block DFE in a 7-nm FinFET wireline receiver. IEEE Journal of Solid-State Circuits. 2022, 57:32-43. 10.1109/jssc.2021.3109167
10. Kim G, Kull L, Luu D, et al.: A 161-mW 56-Gb/s ADC-based discrete multitone wireline receiver data-path in 14-nm FinFET. IEEE Journal of Solid-State Circuits. 2020, 55:38-48. 10.1109/jssc.2019.2938414
11. Vallabhuni RR, Sravya DVL, Shalini MS, Maheshwararao GU: Design of comparator using 18nm FinFET technology for analog to digital converters. 2020 7th International Conference on Smart Structures and Systems (ICSSS), Chennai, India. IEEE, 2020. 1-6. 10.1109/ICSSS49621.2020.9202164
12. Naghizade S, Saghaei H: An ultra-fast optical analog-to-digital converter using nonlinear X-shaped photonic crystal ring resonators. Optical and Quantum Electronics. 2021, 53:149.
13. Martens E, Hershberg B, Craninckx J: A 69-dB SNDR 300-MS/s two-time interleaved pipelined SAR ADC in 16-nm CMOS FinFET with capacitive reference stabilisation. IEEE Journal of Solid-State Circuits. 2018, 53:1161-171. 10.1109/jssc.2017.2784762
14. Lin H, Boecker C, Hossain M, et al.: A 4× 112 Gb/s ADC-DSP based multistandard receiver in 7nm FinFET. 2020 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA. IEEE, 2020. 1-2. 10.1109/VLSICircuits18222.2020.9162802
15. Liang Y, Zhu Z, Li X, Gupta SK, Datta S, Narayanan V: Utilisation of negative-capacitance FETs to boost analog circuit performances. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2019, 27:2855-860. 10.1109/tvlsi.2019.2932268
16. Erdmann C, Verbruggen B, Vaz B, et al.: A modular 16nm direct-RF TX/RX embedding 9GS/S DAC and 4.5 GS/S ADC with 90dB isolation and sub-80PS channel alignment for monolithic integration in 5G base-station SoC. 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA. IEEE, 2018. 219-20. 10.1109/VLSIC.2018.8502292
17. Lee J, Lim Y, Lee J, et al.: A 0.56-mW 63.6-dB SNDR 250-MS/s two-step SAR ADC in 8-nm FinFET. IEEE Solid-State Circuits Letters. 2022, 5:256-59. 10.1109/lssc.2022.3217153
18. Zhang M, Chan CH, Zhu Y, Martins RP: A 0.6-V 13-bit 20-MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed-enhanced techniques. IEEE Journal of Solid-State Circuits. 2019, 54:3396-409. 10.1109/jssc.2019.2938450
19. Upadhyaya P, Poon CF, Lim SW, et al.: A fully adaptive 19-to-56Gb/s PAM-4 wireline transceiver with a configurable ADC in 16nm FinFET. 2018 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA. IEEE, 2018. 108-10. 10.1109/ISSCC.2018.8310207
20. Vaz B, Verbruggen B, Erdmann C, et al.: A 13Bit 5GS/S ADC with time-interleaved chopping calibration in 16NM FinFET. 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA. IEEE, 2018. 99-100. 10.1109/VLSIC.2018.8502306
21. Reddy MCS: Implementation of Pipelined ADC using 22 nm FinFET Technology. i-Manager's Journal on Circuits & Systems. 2021, 9:16.
22. Watanabe T: All-digital VCO-ADC TAD using 4CKES-type in 16-nm FinFET CMOS for technology scaling with stochastic-ADC method. 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Dubai, United Arab Emirates. IEEE, 2021. 1-4. 10.1109/ICECS53924.2021.9665567
23. Yoo BJ, Lim DH, Pang H, et al.: A 56Gb/s 7.7 mW/Gb/s PAM-4 wireline transceiver in 10nm FinFET using MM-CDR-Based ADC timing skew control and low-power DSP with approximate multiplier. IEEE, 2020. 122-24. 10.1109/ISSCC19947.2020.9062964
24. Zhu Y, Liu T, Kaile SK, et al.: A 38GS/s 7b Time-Interleaved Pipelined-SAR ADC with Speed-Enhanced Bootstrapped Switch in 22nm FinFET. 2022 IEEE Custom Integrated Circuits Conference (CICC), Newport Beach, CA, USA. IEEE, 2022. 1-2. 10.1109/CICC53496.2022.9772785
25. Kull L, Luu D, Menolfi C, et al.: A 24-72-GS/s 8-b time-interleaved SAR ADC with 2.0-3.3-pJ/conversion and

>30 dB SNDR at nyquist in 14-nm CMOS FinFET. IEEE Journal of Solid-State Circuits. 2018, 53:3508-516. 10.1109/jssc.2018.2859757

26. Wang A, Shi CJR: A 10-bit 50-MS/s SAR ADC with 1 fJ/conversion in 14 nm SOI FinFET CMOS . Integration. 2018, 62:246-57. 10.1016/j.vlsi.2018.03.010
27. Im J, Zheng K, Chou CHA, et al.: A 112-Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR ADC and Inverter-Based RX Analog Front-End in 7-nm FinFET. IEEE Journal of Solid-State Circuits. 2021, 56:7-18. 10.1109/jssc.2020.3024261
28. Pisati M, De Bernardinis F, Pascale P, et al.: A sub-250mW 1-to-56Gb/s continuous-range PAM-4 42.5 dB IL ADC/DAC-based transceiver in 7nm FinFET. 2019 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA. IEEE, 2019. 116-18. 10.1109/ISSCC.2019.8662428
29. Nguyen RL, Castrillon AM, Fan A, et al.: A Highly Reconfigurable 40-97GS/s DAC and ADC with 40GHz AFE Bandwidth and Sub-35fJ/conv-step for 400Gb/s Coherent Optical Applications in 7nm FinFET. 2021 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA. IEEE, 2021. 64:136-38. 10.1109/ISSCC42613.2021.9365746
30. Baek S, Jang I, Choi M, Roh H, Lim W, Cho Y, Shin J: A 12b 600MS/s Pipelined SAR and 2x-Interleaved Incremental Delta-Sigma ADC with Source-Follower-Based Residue-Transfer Scheme in 7nm FinFET. 2021 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA. IEEE, 2021. 64:172-74. 10.1109/ISSCC42613.2021.9366051
31. Watanabe T: All-digital VCO-ADC TAD confirming scaling and stochastic effects using 16-nm FinFET CMOS. 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Dubai, United Arab Emirates. IEEE, 2021. 1-4. 10.1109/ICECS53924.2021.9665569
32. Kim H, Lee S, Kim J: A 9-Bit 500-ms/s 4-Stage Pipelined SAR ADC With Wide Input Common-Mode Range Using Replica-Biased Dynamic Residue Amplifiers. IEEE Access. 2023, 11:22531-2541. 10.1109/access.2023.3248784
33. Aiello O, Crovetti P, Alioto M: Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation. IEEE Access. 2020, 8:70890-899. 10.1109/access.2020.2986949
34. Srivastav A, Tiwari U, Mandal SK, Sachdeva A: A FinFET-based low leakage 10T static random access memory cell. Journal of Circuits Systems and Computers. 2024, 34:10.1142/s0218126625500975