Cureus Journal of Engineering

Open Access Original Article

Impact of Temperature on Radio Frequency and Analog Performance of High-K Dual-Metal and Dielectric-Pocket Nanotube Field-Effect Transistors (FETs)

Received 08/31/2025
Review began 09/23/2025
Review ended 11/24/2025
Published 12/17/2025

DOI:
https://doi.org/10.7759/s44388-025-09914-8

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Abstract

This article presents a detailed comparative analysis of the analog and radio frequency (RF) performance of HK-DM-NTFETs and HK-DP-NTFETs across a temperature range of 250 K to 400 K. The high-k (HK) dielectric improves the on-state saturation current, reduces gate leakage, and minimizes self-heating effects, while structural innovations such as dielectric pocket (DP) and dual-metal (DM) configurations are employed to further optimize device behavior. The DP structure is effective in suppressing off-state leakage current and enhancing electrostatic control, whereas the DM configuration primarily improves short-channel effects such as drain-induced barrier lowering and sub-threshold swing.

Simulation results, obtained using a calibrated TCAD device simulator, demonstrate that HK-DP-NTFETs consistently outperform their HK-DM counterparts across all operating temperatures. The HK-DP device exhibits ~13% higher drain current, ~50% lower gate capacitance, and superior cut-off frequency performance, resulting in enhanced drive capability, reduced capacitive delay, and better high-frequency response. Moreover, the HK-DP structure maintains its advantages under elevated temperatures, indicating stronger thermal resilience. These findings firmly establish HK-DP-NTFETs as the superior architecture for achieving robust analog and RF performance in future nanoscale applications.

Categories: Electronics Design and VLSI, Nanoelectronics and Quantum Computing, Nanotechnology
Keywords: cut-off frequency, nanotube, gate capacitance, nanowire, dual-metal, dielectric pocket

Introduction

The "International Roadmap for Devices and Systems (IRDS)" highlights nanotube-shaped Field-Effect Transistors (FETs) as a leading approach for addressing short channel effects (SCEs) in technology nodes below 7 nm [1,2]. Prominently, several major semiconductor foundries are anticipated to achieve the 3 nm node by the end of the year [3]. Comparative analysis by H.M. Fahad reveals that tubular architectures outperform wire-like FETs by delivering twice the drive current and significantly reducing inverter delay [4]. These cylindrical designs exhibit enhanced electrostatic control [5] and are also referred to as double-gate-all-around (DGAA) FETs [6].

Device performance can be significantly improved through the integration of high-k dielectrics, dielectric pockets (DP), and multi-metal gate architectures. Encasing gates with high-k dielectrics has been demonstrated to enhance key parameters such as on-current (Ion), trans-conductance (g_m), gate delay, and the trans-conductance generation factor [7]. Mahindhar et al. [8] report that high-k-based Nanowire-FETs exhibit superior performance at lower operating temperatures. The incorporation of dielectric pockets at the source/drain (S/D) interface effectively suppresses off-current (I_{off}) by obstructing minority carrier flow paths [9], thereby improving the I_{on}/I_{off} ratio-though a minor reduction in I_{on} may occur [10]. Jurczak et al. [11] successfully applied the DP concept to 0.15µm PMOS devices, referring to the method as insulated shallow extension. Awasthi et al. [12] found that DP integration enhances thermal stability compared to conventional devices, while Purwar et al. [13] observed that DP-DGAA MOSFETs show reduced mobility degradation under temperature stress. The Dual-Metal-Gate (DMG) strategy, first introduced by Long et al. in 1999 [14], utilizes control and screen gates to strengthen n-channel MOSFET performance, offering improved immunity to SCEs and mitigating hot-carrier injection and drain-induced barrier lowering.

Despite extensive prior research, temperature-dependent comparative analyses of various analog/radio frequency (RF) performance parameters for HK-DM-NTFET and HK-DP-NTFET remain unexplored. This

How to cite this article
Jaiswal K, Purwar V, Dixit M K, et al. (December 17, 2025) Impact of Temperature on Radio Frequency and Analog Performance of High-K Dual-Metal and Dielectric-Pocket Nanotube Field-Effect Transistors (FETs) . Cureus J Eng 2 : es44388-025-09914-8. DOI https://doi.org/10.7759/s44388-025-09914-8

study bridges that gap by evaluating these structures under varying thermal conditions, offering valuable insights into device reliability and operational lifespan. Additionally, the findings contribute to improved thermal management strategies during integrated circuit fabrication. All simulations were conducted using the Silvaco TCAD tool to identify the most temperature-resilient device architecture.

Materials And Methods

S. No.	Parameter	Device simulation/calibration parameters	
		DM-NTFET	DP-NTFET
i	**Channel length (L)**	**30 nm**	**30 nm**
ii	Source/Drain Doping (Ns,Nd)	10^{20} cm^{-3}	10^{20} cm^{-3}
iii	Channel Doping (N_A)	10^{15} cm^{-3}	10^{15} cm^{-3}
iv	Thickness of the oxide (t_{ox})	1 nm	1 nm
v	High K Thickness (HfO2)	1 nm	1 nm
vi	Thickness of the channel (t_{si})	10 nm	10 nm
vii	Core gate radius	4 nm	4 nm
viii	Work-function of the metal-1 (ϕ_{m1})	4.9eV	4.79eV
ix	Work-function of the metal-2 (ϕ_{m2})	4.61eV	---
x	Dielectric pocket length (DP_L)	---	5 nm
xi	Dielectric pocket thickness (DP_T)	---	6 nm

TABLE 1: Dimensions of HK-DM-NTFET and HK-DP-NTFET for simulation

HK, high-k; DM, dual-metal; DP, dielectric pocket

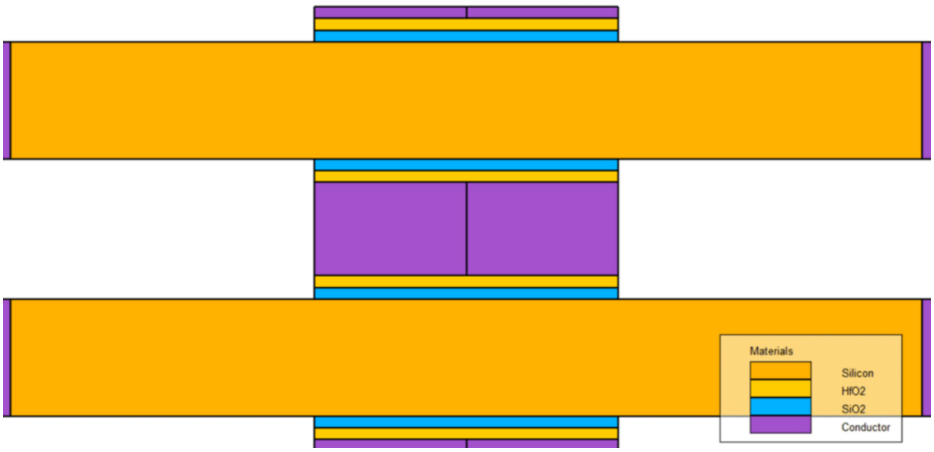

FIGURE 1: Sectional view of HK-DM-NTFET

HK, high-k; DM, dual-metal

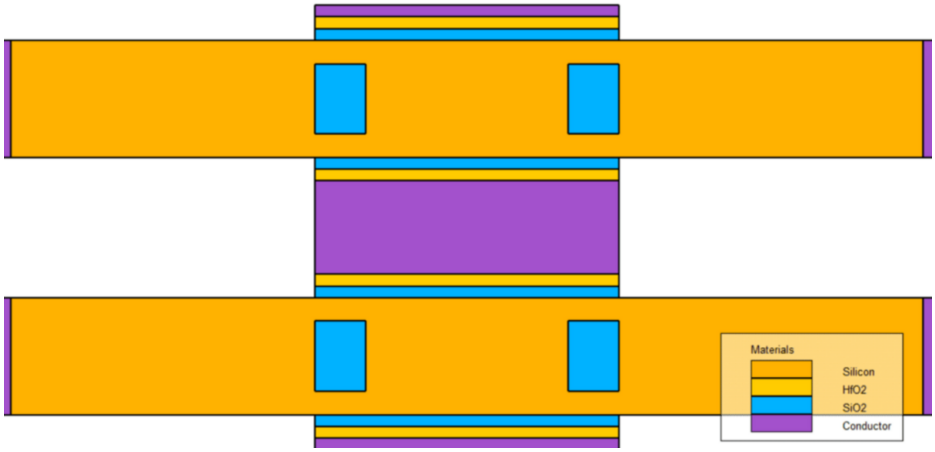

FIGURE 2: Sectional view of HK-DP-NTFET

HK, high-k; DP, dielectric pocket

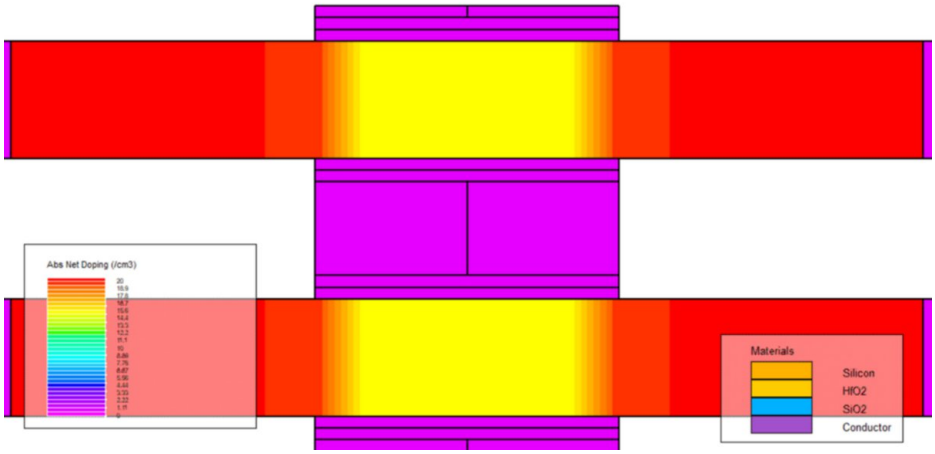

FIGURE 3: Contour plot of HK-DM FETs

HK, high-k; DM, dual-metal; FET, Field-Effect Transistors

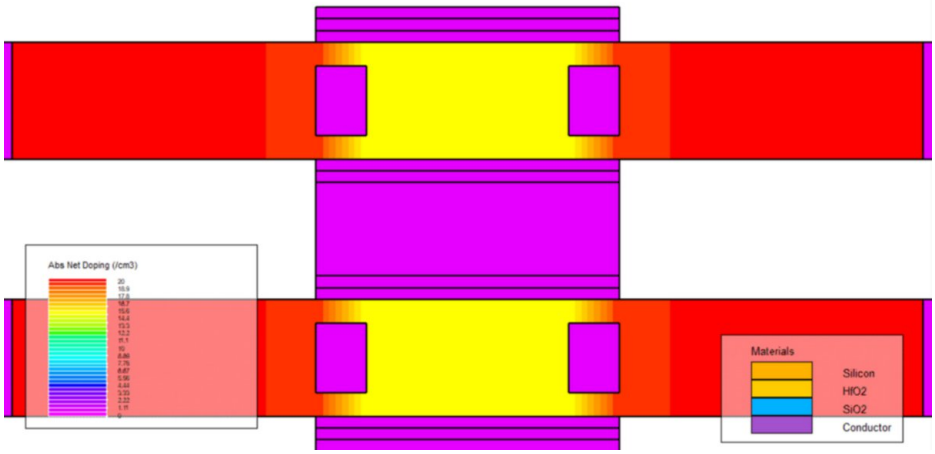

FIGURE 4: Contour plot of HK-DP FETs

HK, high-k; DP, dielectric pocket; FETs, Field-Effect Transistors

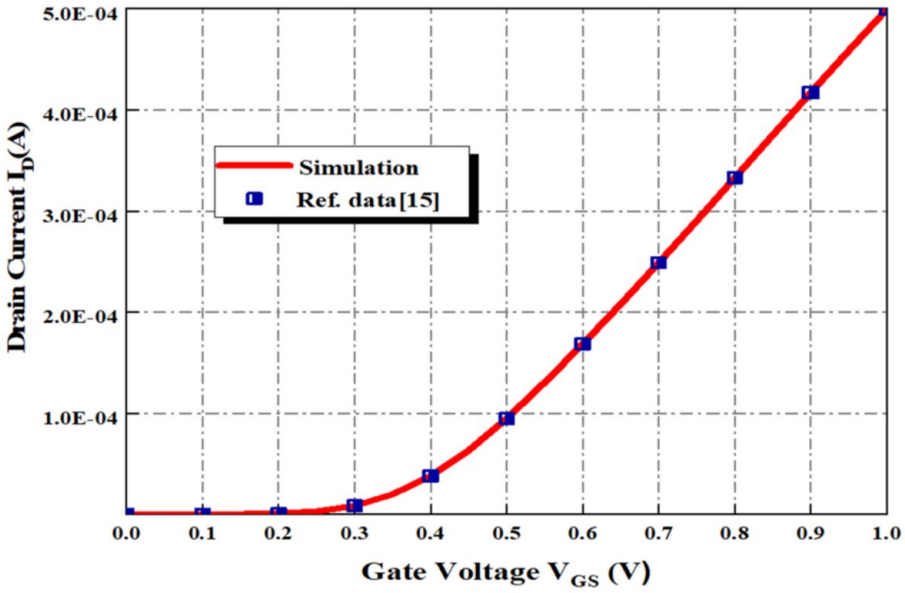

FIGURE 5: Comparison of Drain current (ID) from simulation with experimental Ref. data

Figures *1* and 2 present the cross-sectional views of the HK-DM-NTFET and HK-DP-NTFET structures, respectively. In both configurations, silicon dioxide (SiO_2) and hafnium oxide (HfO_2) layers encase the cylindrical channel, as depicted in the two-dimensional schematic. The DP design features two oxide pockets symmetrically positioned near the source and drain ends of the channel. In contrast, the DM architecture incorporates two sequentially stacked metal gates above the dielectric, maintaining a 1:1 thickness ratio. The metals utilized here are tungsten disilicide and zinc. Figures *3* and 4 show the contour plot of HK-DM and HK-DP devices.

The entire simulation has been done on Silvaco TCAD simulation software. For simulation purposes, a combination of Drift-Diffusion, High-Field Saturation, and Concentration and Field-Dependent methods has been employed. Simulation software will generate the various device parameters in a CVC file. With the help of this data, various graphs have been plotted in Origin software. The associated simulation and calibration parameters are detailed in Table *1*. Figure *5* illustrates the alignment between experimentally obtained ref. data [15] and their simulated counterparts [13]. This calibration graph justifies that predicted values by the simulator are close to the fabricated device. Quantum confinement effects are considered negligible for the chosen device dimensions, as supported by reference [16].

Results And Discussion

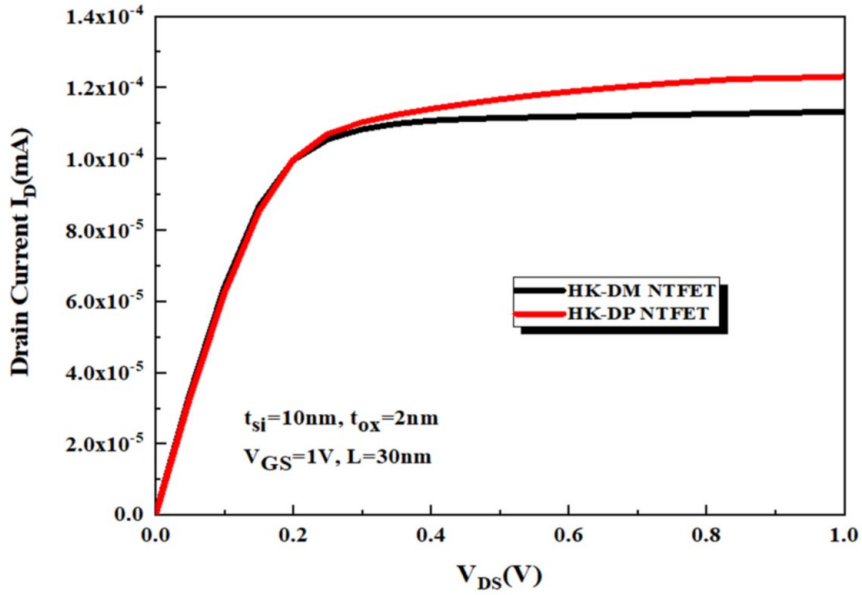

FIGURE 6: The variation of Drain Current (ID) against drain-to-source Voltage (VDS)

Figure *6* illustrates how the drain current varies with drain voltage (V_{DS}) at a gate voltage (V_{GS}) of 1 volt, with device parameters L = 30 nm, t_{si} = 10 nm, and t_{ox} = 2 nm. Both devices reflect a similar pattern in the linear region, while after pinch-off, the HK-DP-NTFET achieves a noticeably higher saturation current compared to the HK-DM-NTFET. For HK-DP-NTFET, the increase in saturation current is 63%, and for HK-DM-NTFET, it is 49.9% as compared with NTFETs. The rise in saturation current in the HK-DP structure demonstrates its superior current drive capability, which arises from improved carrier transport enabled by dielectric pocket engineering.

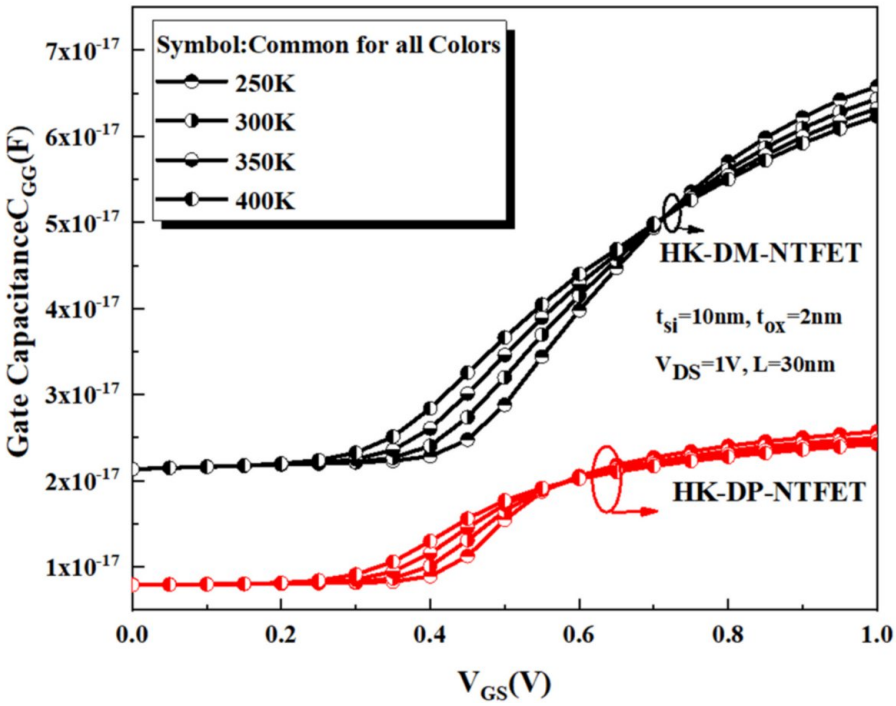

FIGURE 7: Gate capacitance CGG vs VGS variation for different temperatures

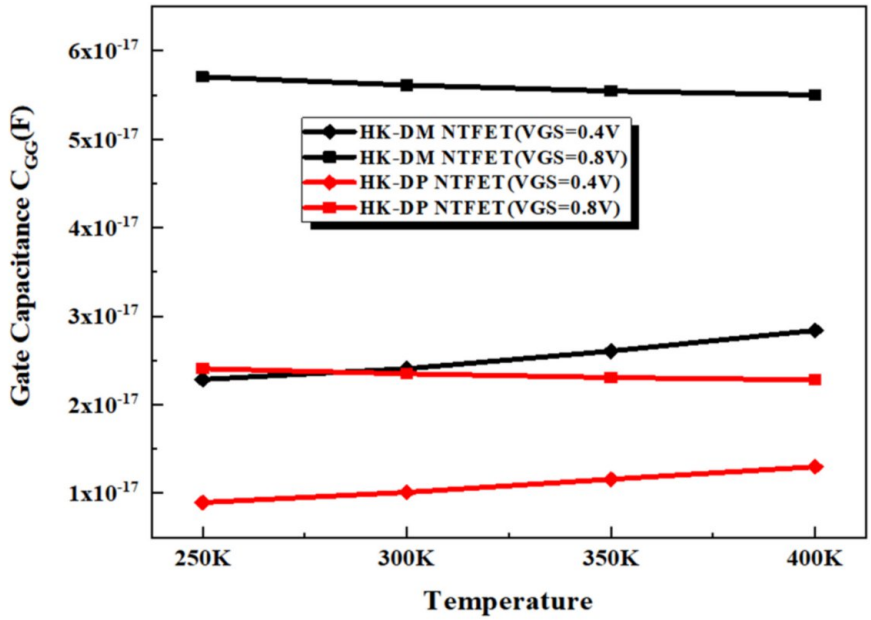

FIGURE 8: Gate capacitance CGG vs temperatures (below/above threshold voltage)

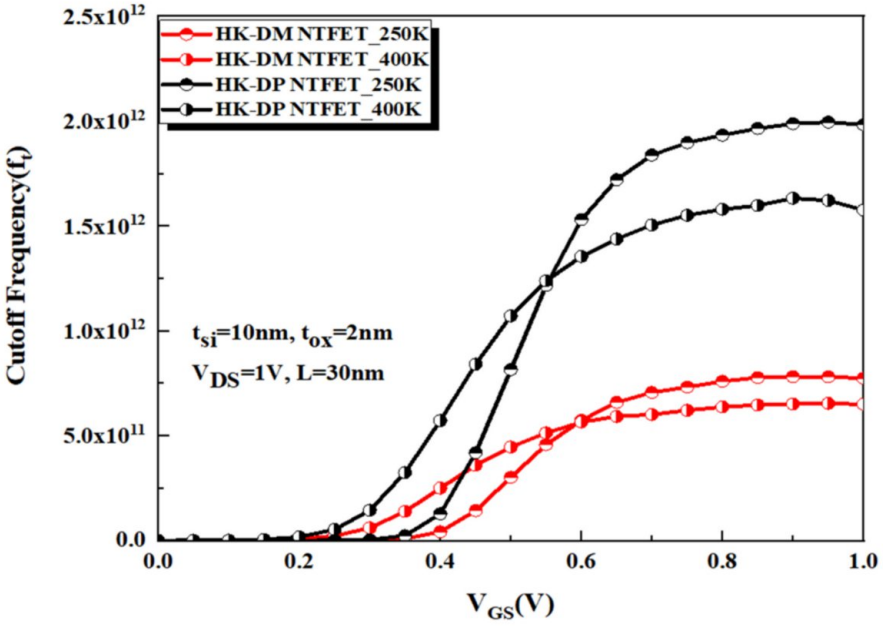

FIGURE 9: Cutoff frequency (ft) vs VGS variation for different temperatures

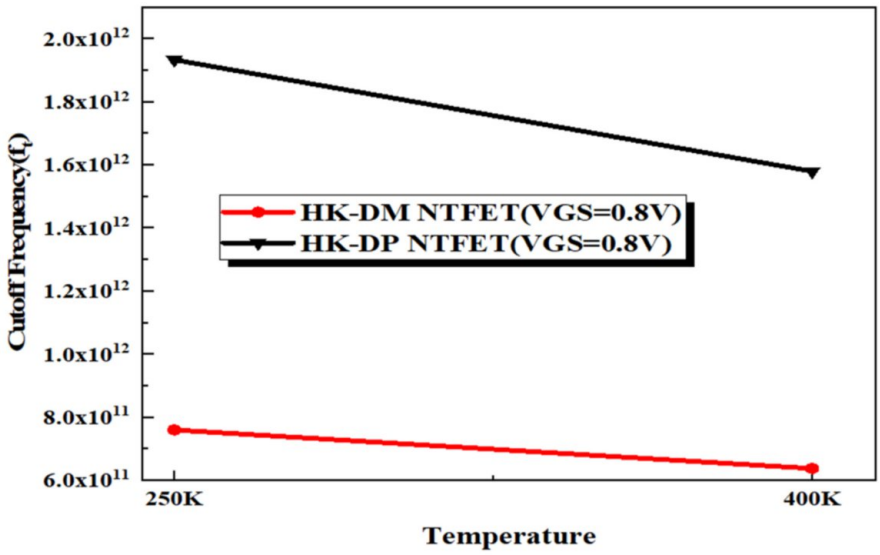

FIGURE 10: Cutoff frequency (ft) vs temperatures at VGS = 0.8 V

The HK-DP-NTFET optimizes the saturation current at standard room temperature (300 K) by 13% as compared with HK-DM-NTFETs.

Figure 7 shows the variation of gate capacitance (C_{GG}) with gate-to-source voltage (V_{GS}) for HK-DM-NTFET and HK-DP-NTFETs across the temperature range of 250 K to 400 K at V_{DS} = 1 V. The total gate capacitance, given by $C_{GG} = C_{GS} + C_{GD}$, is evaluated by superimposing a small AC signal over the DC gate bias. It is observed that HK-DM-NTFETs consistently exhibit higher C_{GG} values (above 6×10^{-17} F at higher V_{GS}), while HK-DP-NTFETs maintain much lower capacitance levels (around 2×10^{-17} F). The reduced capacitance in HK-DP devices arises from the dielectric pocket, which effectively minimizes fringing fields and weakens gate-to-channel coupling. Moreover, HK-DP-NTFETs demonstrate reduced temperature dependence, making their capacitance behavior more stable across operating conditions.

These results highlight that although HK-DM-NTFETs exhibit higher capacitance, the HK-DP structure is superior for analog/RF applications, as its lower C_{GG} directly translates to reduced parasitic effects, improved scalability, and enhanced high-frequency device performance.

Figure *8* covers the variation of gate capacitance against various temperatures for below threshold voltage (V_{GS} = 0.4V) and above threshold voltage (V_{GS} = 0.8V). Below the threshold voltage on increasing the temperature, gate capacitance shows an increasing behavior, while above the threshold voltage, the converse is reflected in the figure. On increasing the temperature, HK-DM-NTFET produces higher gate capacitance when compared to the HK-DP-NTFET structure. The straightness of all these graphs reflects the immunity toward temperature, and HK-DP-NTFET produces the highest immunity against temperature.

Figure *9* illustrates the variation of cutoff frequency (f_t) with respect to V_{GS} at temperatures of 250 K and 400 K, with V_{DS} = 1 V. The cutoff frequency, which serves as a key parameter for evaluating the RF performance of FET devices, f_t represents the point at which the current gain becomes unity and is calculated as $g_m/2pi*C_{GG}$. As the temperature decreases, the crossover point for achieving higher V_{GS} values shifts forward, reflecting the influence of thermal effects on carrier transport. Furthermore, owing to its smaller gate capacitance (C_{GG}), the HK-DP-NTFET reflects a higher f_t, while the HK-DM-NTFET exhibits a comparatively lower one, confirming the performance advantage of the dielectric pocket structure.

Figure *10* depicts the variation of cutoff frequency (f_t) with temperature for HK-DM-NTFET and HK-DP NTFET at V_{GS}=0.8V. As the temperature increases from 250 K to 400 K, both devices exhibit a reduction in f_t due to enhanced phonon scattering and carrier mobility degradation; however, the extent of this variation is significantly higher in the HK-DM-NTFET, while the HK-DP-NTFET shows a comparatively smaller decrease. This behavior indicates that the dielectric pocket structure not only provides a higher cut-off frequency but also makes the device more immune to temperature variations in terms of f_t , thereby ensuring superior thermal stability and high-frequency performance compared to the double-material design.

Conclusions

The analog/RF performance evaluation of HK-DM-NTFET and HK-DP NTFET across a wide temperature range (250-400 K) clearly establishes the superiority of the HK-DP architecture. The HK-DP-NTFET consistently demonstrates ≈13% higher saturation drain current, which improves transconductance and drive capability. In addition, it exhibits a significantly lower gate capacitance (CGG), thereby reducing parasitic effects and enhancing device scalability. As a result, the cut-off frequency as $f_t = g_m/2\pi C_{GG}$ is notably higher in the HK-DP device compared to HK-DM, highlighting its advantage for high-frequency RF applications. Furthermore, HK-DP shows better thermal stability, with reduced sensitivity of current, capacitance, and cutoff frequency to temperature variations. Collectively, these characteristics-higher saturation current, lower capacitance, enhanced f_t, and stronger immunity against temperature effects-make the HK-DP-NTFET the most suitable structure for advanced nanoscale and high-performance analog/RF circuits.

Additional Information

Author Contributions

All authors have reviewed the final version to be published and agreed to be accountable for all aspects of the work.

Concept and design: Vaibhav Purwar, Kaushik Jaiswal, Manish K. Dixit, Manish Tiwari, Chetan Sambhajirao More

Acquisition, analysis, or interpretation of data: Vaibhav Purwar, Kaushik Jaiswal, Manish K. Dixit, Manish Tiwari, Chetan Sambhajirao More

Drafting of the manuscript: Vaibhav Purwar, Kaushik Jaiswal, Manish K. Dixit, Manish Tiwari, Chetan Sambhajirao More

Critical review of the manuscript for important intellectual content: Vaibhav Purwar, Kaushik Jaiswal, Manish K. Dixit, Manish Tiwari, Chetan Sambhajirao More

Supervision: Vaibhav Purwar, Kaushik Jaiswal, Manish K. Dixit, Manish Tiwari, Chetan Sambhajirao More

Disclosures

Human subjects: All authors have confirmed that this study did not involve human participants or tissue. **Animal subjects:** All authors have confirmed that this study did not involve animal subjects or tissue. **Conflicts of interest:** In compliance with the ICMJE uniform disclosure form, all authors declare the following: **Payment/services info:** All authors have declared that no financial support was received from any organization for the submitted work. **Financial relationships:** All authors have declared that they have no financial relationships at present or within the previous three years with any organizations that might have an interest in the submitted work. **Other relationships:** All authors have declared that there are no other relationships or activities that could appear to have influenced the submitted work.

Acknowledgements

This article was previously presented at the International Conference on NEXT GENERATION TECHNOLOGY IN SCIENCE AND ENGINEERING (ICNGTSE - 2025) at Pranveer Singh Institute of Technology, Kanpur (PSIT) on 22nd – 23rd August 2025.

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